Appendix C

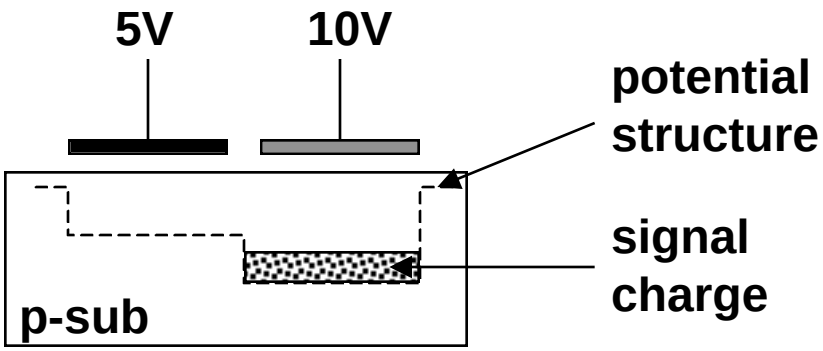
Other Imager Types

Charge Injection Devices

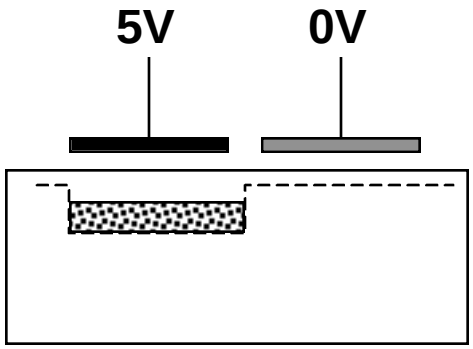
- **Charge injection devices lie somewhere between CCDs and photogates**
  - » they the employ X-Y addressing of CMOS arrays
  - » but two stages of charge transfer that is more like a CCD structure
- **For this reason, CIDs are not usually considered to be true CMOS devices**
- **One of the unique features of this technology is the ability to perform non-destructive readout of the the signal**
  - » in which case, the same signal can be read out several times, and averaged
  - » this averaging process reduces random noise by a factor of $1/\sqrt{N}$, where N is the number of signals averaged
  - » the limits to this are the time required for the multiple readout and the limitation of dark current
- **Each pixel of the CID consists of two MOS capacitors**
  - » connected either by overlapping gates or a bridging diffusion ...

CID Pixel

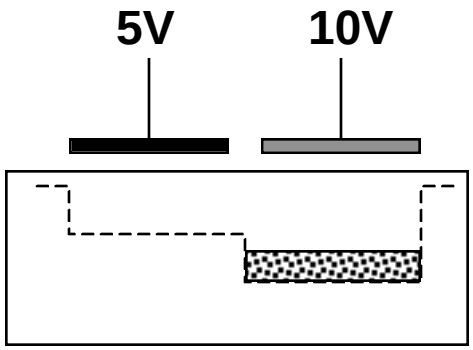
- **Integration period:**



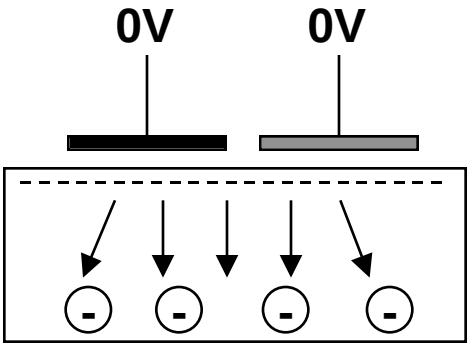
- **Non-destructive readout:**



- **Continued signal integration:**



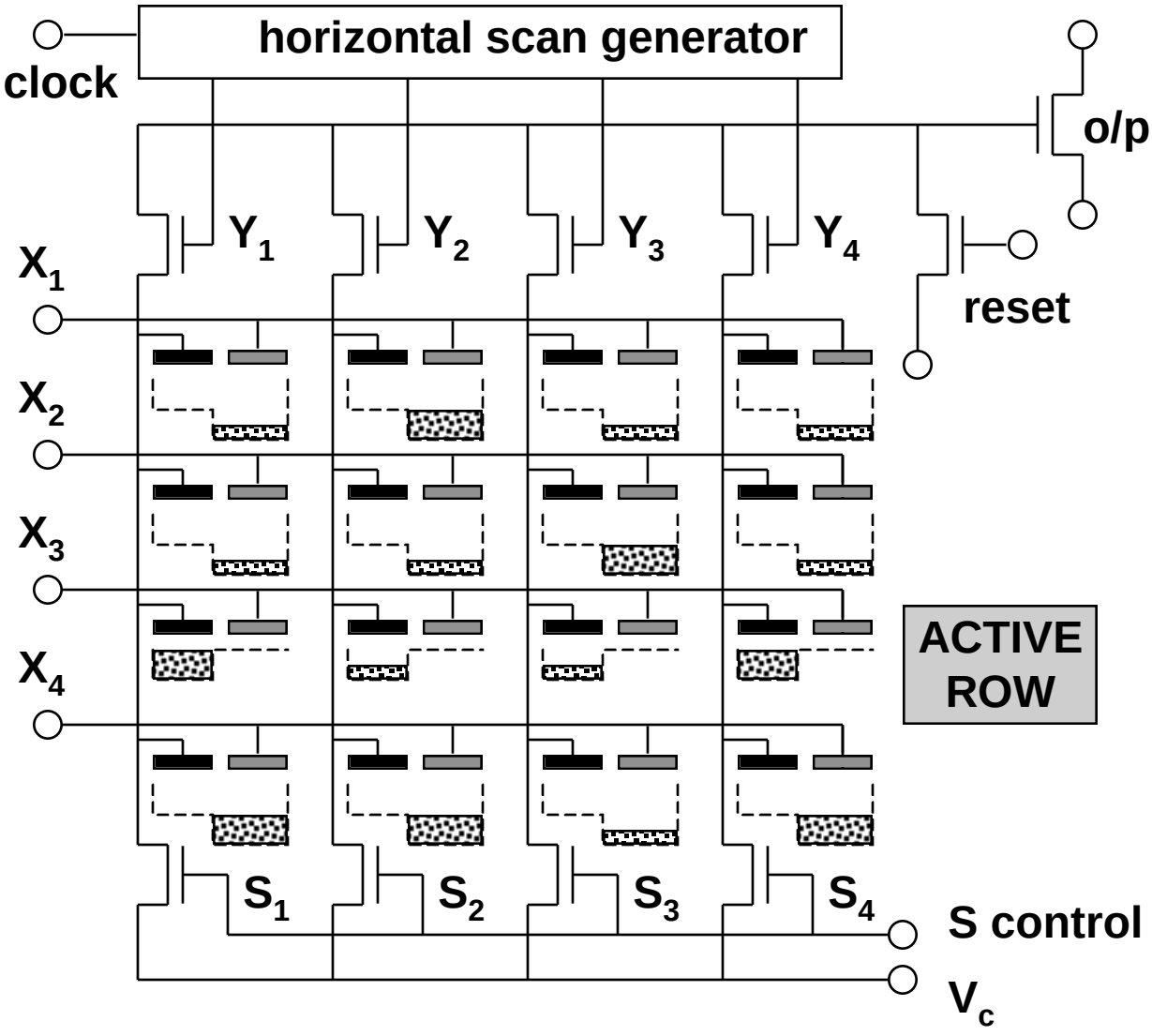
- **Charge dumping**



- **This charge dumping is accomplished by <u>injecting</u> the minority electrons into the substrate**
- **Since this is effectively discharging the MOS capacitors**
  - » a displacement current will flow
  - » the size of which depends on the amount of charge injected
  - » which is a function of the illumination
- **In early devices, this displacement current was measured as the output signal**
  - » hence the name, charge injection device
- **More recent devices detect the change of capacitance of the output electrodes**
  - » the array structure is shown below

CID Array Architecture

- CID pixels are arranged in an X-Y addressed array



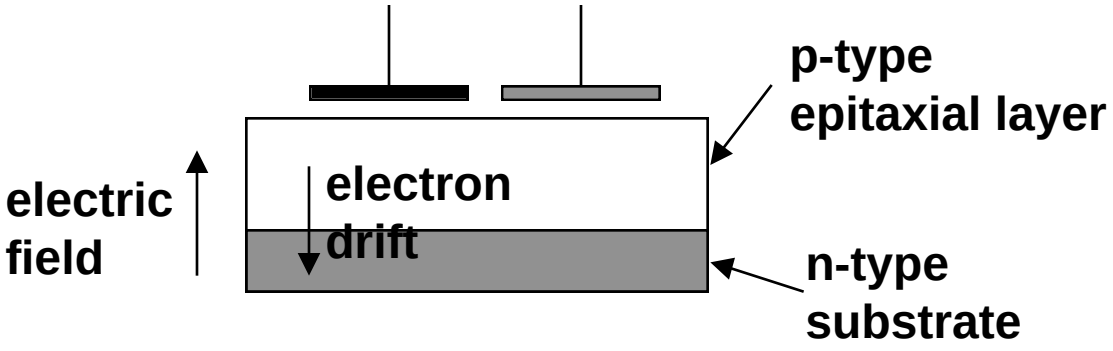
- Here, X_3 is the active row

CID Array Readout

- **Initially, all columns are set to their reference voltage (e.g. 5V) through $S_{1\text{-}4}$**
  - » and then left floating with $S_{1\text{-}4}$ open
- **Voltages on $X_{1\text{-}4}$ are maintained higher than on the columns (e.g. 10V)**
  - » this keeps the signal charge in unaddressed wells from influencing the column voltages
- **A row is activated by setting its voltage to zero**
  - » thereby moving the charge to the column electrodes
- **Each of the column voltages will change by an amount Q_{signal}/C_{column}**
  - » and these are then read out via $Y_{1\text{-}4}$
  - » after this, the output is reset
- **For high-speed applications, the activated row can now be reset simultaneously by pulsing each column to zero**
  - » dumping the charge into the substrate
  - » subsequently, the columns are returned to 5V
- **Alternatively, the original voltages can be restored, and the integration is continued**

Charge Injection

- **Dumping the charge into the substrate requires a fast recombination**
  - » to avoid image lag and crosstalk between pixels
- **But this is contrary to the requirements for high minority carrier lifetimes imposed by the deep depletion of the MOS capacitors**
- **The solution is to add a p-n junction in the substrate to sweep away the charges**
  - » to recombine at their leisure

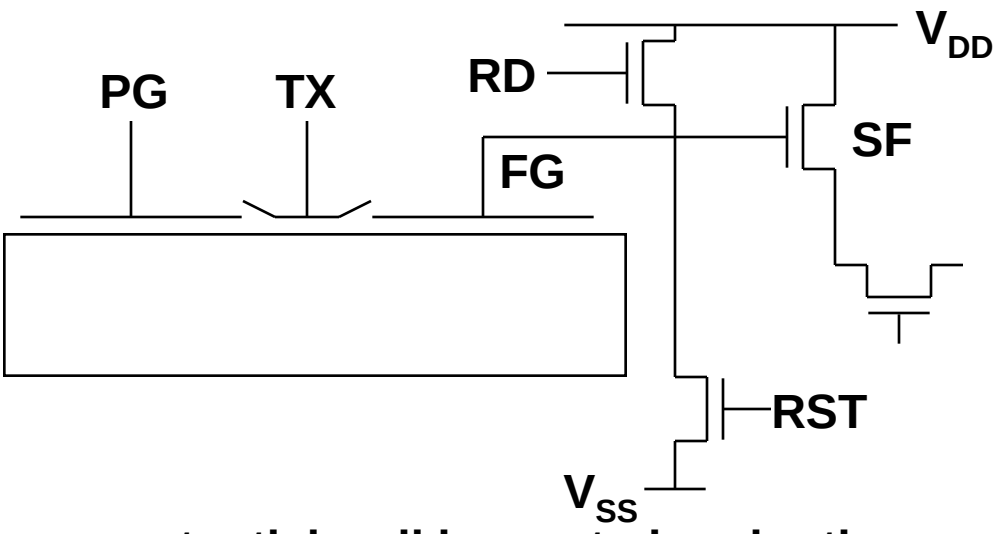


- **This also serves as an blooming reduction device**

CID Performance

- **The CID structure has several advantages**
  - » no requirement for buried channel etc because there is only one charge transfer
  - » random accessibility
  - » high fill factor
  - » integration
  - » non-destructive readout
- **And one major disadvantage**
  - » high bus capacitance leads to low conversion efficiency and high noise levels
  - » these can be mitigated by averaging, but readout time and dark current limit the extent to which this can be used
- **One solution to the capacitance problem is to make the CID effectively an active pixel device**
  - » by inserting a buffer between the column electrode and the column
  - » thus making that electrode into a floating gate
- **This completes the "family" of CCD-type CMOS pixels**

CID with Floating Gate



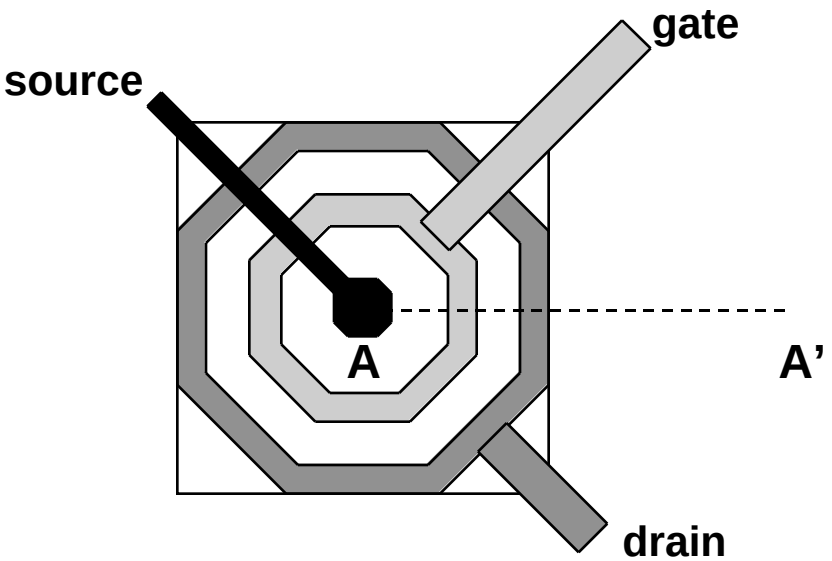
- **Here, a potential well is created under the floating gate (FG) by the RD transistor**
- **Then the integrated charge is transferred to FG by collapsing the well under the photogate (PG)**
- **The change of charge on the FG capacitance is detected as a voltage and output via the source follower (SF)**
- **The output node can then be reset to V_{SS}**
  - » dumping the charge into the substrate
- **Or the charge can be transferred back to the photogate in a non-destructive readout**
- **The TX gate can be replaced by a diffusion, as usual**

Summary of CCD-type Pixels

- **The family of CCD-type imagers can be summarised as follows**
- **True CCD**
  - » CCD imaging element, and CCD readout
  - » discrete conversion node
- **Charge Injection Device**
  - » CCD imaging element, with X-Y addressing
  - » and charge dumping into the substrate
  - » conversion on the bus capacitance
- **Floating Gate CID**
  - » readout gate of CID is separated from the bus capacitance by a MOSFET
  - » conversion node is the floating gate
  - » still reset using charge dumping
- **Floating Diffusion CID = Photogate APS**
  - » readout gate is replaced by a floating diffusion
  - » non-destructive readout is not possible
  - » during reset, electrons are removed to V_{DD} instead of substrate

Charge Modulation Devices

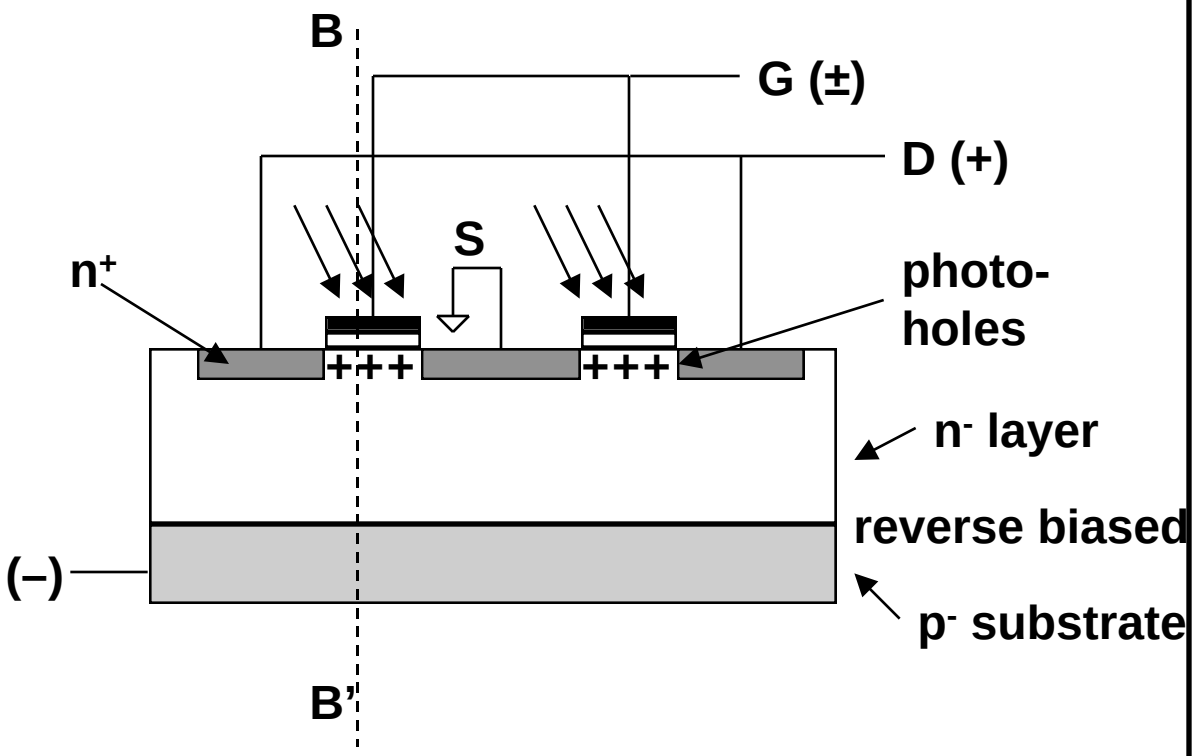
- **The last of the MOS structures is the Charge modulation Device (CMD)**
  - » which is essentially a photo-MOSFET
- **In plan view, the CMD pixel looks like**



- **The idea is that photo-generated holes, collected under the gate of the device, change the effective gate voltage**
  - » and therefore modulate the current flowing in the MOSFET
- **Hence, the device can add internal gain due to the transistor action**

CMD Structure

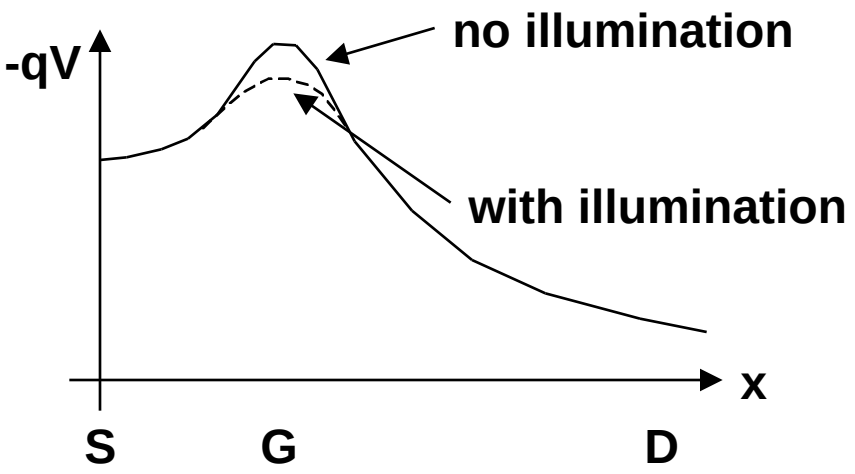
- The concentric rings of the device define a buried channel MOSFET



- The reverse bias on the substrate junction maintains a buried channel in the lightly doped n^- layer
- This separates the electron flow from the photo-generated holes beneath the gate
- Hence the readout is non-destructive

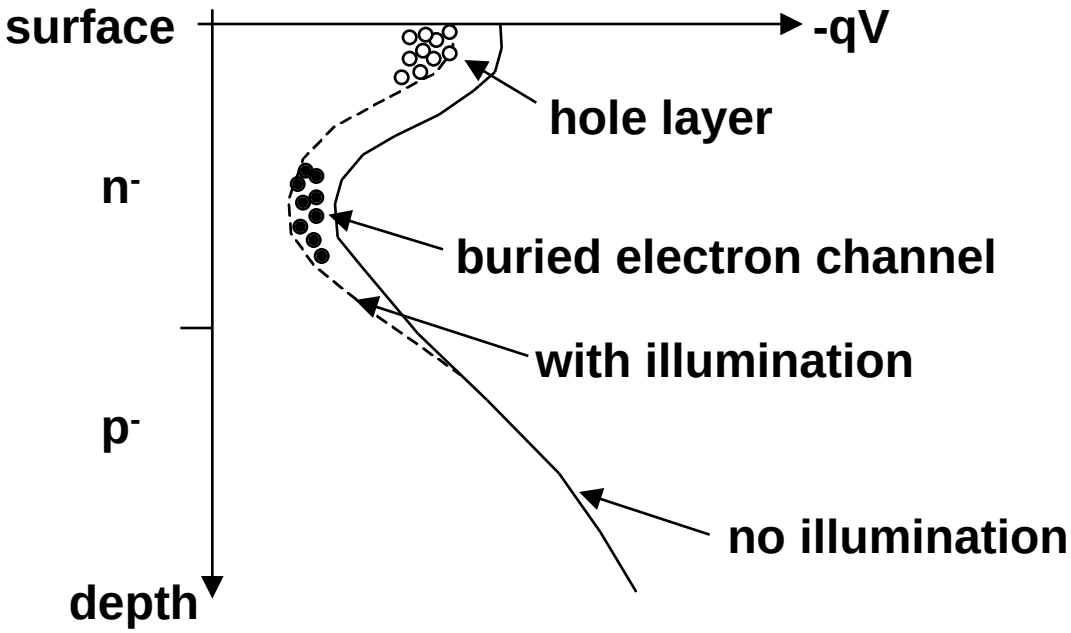
Potential Diagrams

- **Along the line A-A' (p 5.25) the potential looks like**



- **This represents the potential barrier that electron have to overcome between source and drain**
  - » this barrier is lowered by the presence of the photo-generated holes under the gate

- **Along the line B–B' (p 5.26) beneath the gate, the variation of potential with depth is**



- **During integration, V_G is set large & negative**
  - » to create a deep depletion layer for hole integration
  - » and to pinch off the current flow
- **During readout, the V_G is made less negative and V_D is applied**
  - » allowing the readout current to flow
- **When the readout procedure is completed, the holes can be removed by pulsing the gate positive**

Typical Figures

- **The CMD technology was largely developed by Japanese companies for high resolution TV imaging**
  - » particularly Olympus in the mid-1980s
  - » and recently by NHK, the Japanese state TV system
- **Recent papers report 1920x1035 pixel colour cameras, operated at 60Hz frame rate for HDTV applications**
  - » pixels ≤ 7.6μm square have been fabricated
- **To date, CMD devices have exhibited relatively large dark currents and fixed pattern noise**
  - » the FPN due mainly to geometric variations
  - » and high dark current also introduces a source of noise
- **It should be noted that the process of forming the buried channel is not inherently available with the standard CMOS process**
  - » but is compatible
  - » however, the presence of the MOSFET in the pixel does class the CMD as an active pixel sensor

References

» E. Eid (1995), “Pre-amplifier per pixel charge injection device image sensor”, Proc SPIE **2415**, 292

» K. Matsumoto et al. (1985), “A new MOS phototransistor operating in a non-destructive readout mode”, Japan. J. Applied Phys. **24**, L323

» K. Mitani et al (1996), “A 2K x 2K image acquisition system using four CMD imagers”, Proc. SPIE **2663**, 29