Appendix B

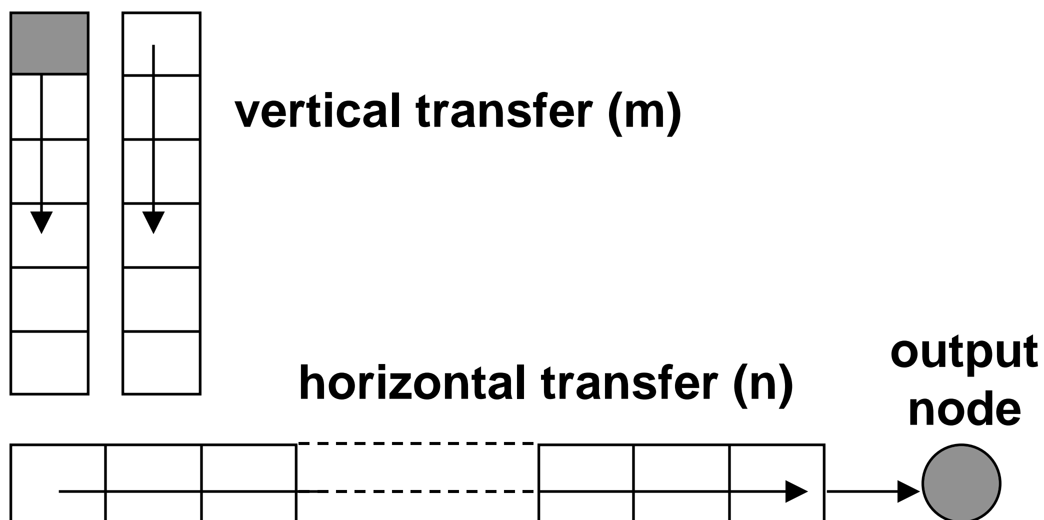
CCD Technology

CCD Operation

- **As we saw in the *Sensors* article, the CCD operated by "pouring" charge from one potential well to the next**
  - » using appropriately pulsed electrodes
- **That article also discussed the ways in which CCD arrays can be scanned**
- **However, it did not really address the implications of the technique**
  - » what we will find is that the CCD needs a number of special features in order to work effectively
  - » this is reasonable; CMOS designs are optimised for low power consumption, speed and flexibility, while CCDs are optimised for CCD imaging
- **The advantages of CCDs include**
  - » large fill factor (no "opaque" transistors)
  - » high sensitivity
  - » low noise levels
  - » large-area formats (e.g. DALSA 4096x4096)

Charge Transfer Efficiency

- **The essential part of the CCD operation is that <u>all the charge</u> must be transferred from gate to gate**
  - » well, 99.999% anyway!
  - » the completeness of this charge transfer is dictated by the number of steps required to get the charge out of the array ...

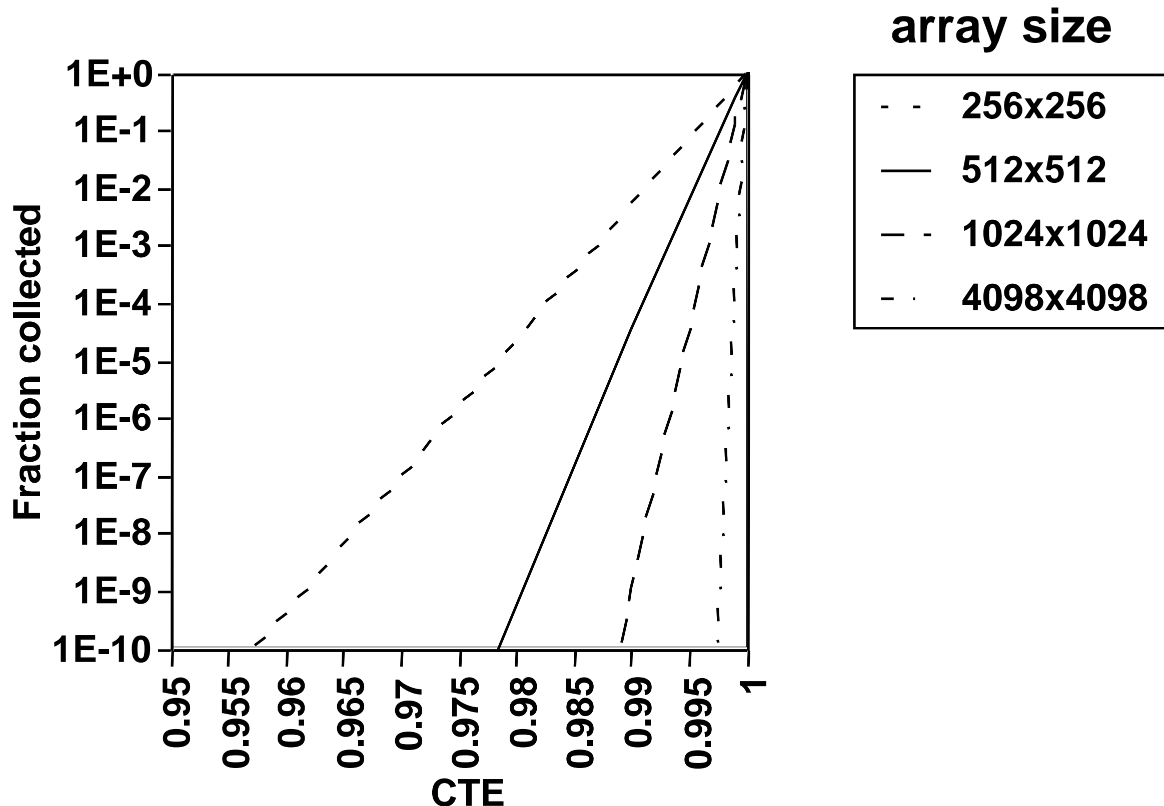


- **We define the <u>charge transfer efficiency</u> ( ) to be the fraction of the well charge that is transferred at each step**
  - » in the worst case, the charge from the shaded pixel above is transferred (n + m) times

- **So the fraction of the original charge that remains is given by**

(n + m)

  » the fraction of the original charge collected as a function of CTE is



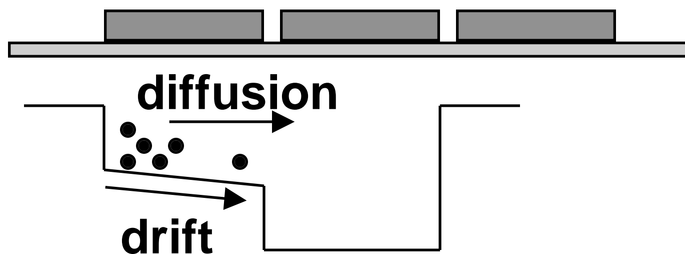
- **CCDs are able to achieve the required charge transfer efficiency**

  » but it needs specialised techniques

  » and it makes the sensor susceptible to, for example, radiation damage

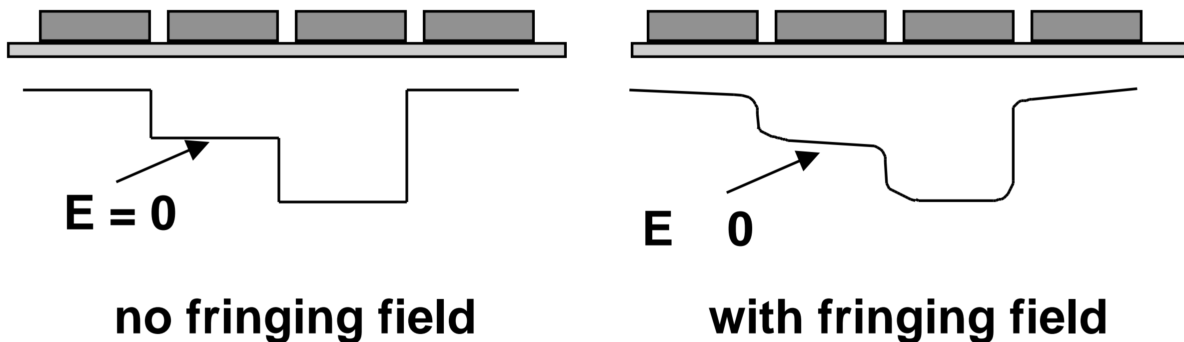
Why is   1?

- **There are two main causes for loss of charge in the transfer**
  » lack of time to complete the transfer
  » charge trapping
- **Of course, this means that the next charge packet may gain charge left behind by the previous one**
- **Charge transfer occurs by a combination of**
  » carrier diffusion
  » carrier drift



- **Charge transfer by carrier diffusion is maximised by**
  » short gates
  » a high diffusion coefficient
  » for electrons in p-type, the diffusion coefficient is about 3x that for holes in n-type

- **The drift is assisted by careful design of the transfer gates**
  - » to achieve a fringing field so that carriers are swept into the next well
  - » the fringing field is larger for lower substrate doping and closer, shorter gates

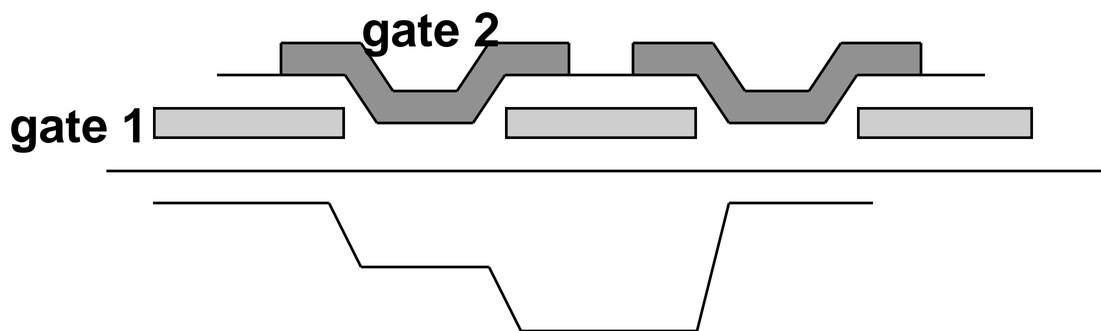


- **So the time required to get 99.99% transfer efficiency as a function of gate length, for 3 substrate doping levels (i.e. fringing fields), is**

Yang fig 13.10

Overlapping Gates

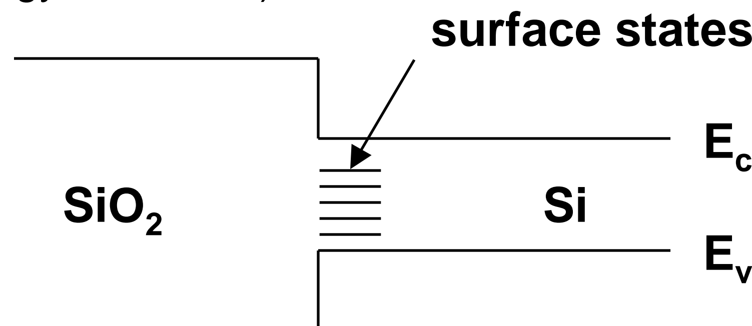
- **The requirement for gates that are closer together (to assist fringing fields) is tough to meet**
  - » the spacing must be sub-micron
  - » but CCD processes usually have feature sizes of 2µm or so (because of large area, deep diffusions etc)
- **Therefore gates are made so that they are overlapping**



- **Such a process requires the deposition of at least two separate layers of poly-Si gates**
  - » unlike a conventional digital CMOS process which uses only one
  - » and appropriate isolation processing

Charge Trapping

- **Charge trapping causes electrons to get “stuck” in the well**
  - » thereby removing them from one charge packet
  - » and releasing them at into another packet at a later time
  - » they cause both transfer inefficiency and image lag
- **Trapping occurs because there are defects in the c-Si at the interface with the SiO_2**
  - » energy levels are created within the Si bandgap
  - » electrons “fall” into these traps
  - » the only way out is back up again (may be a large energy difference)



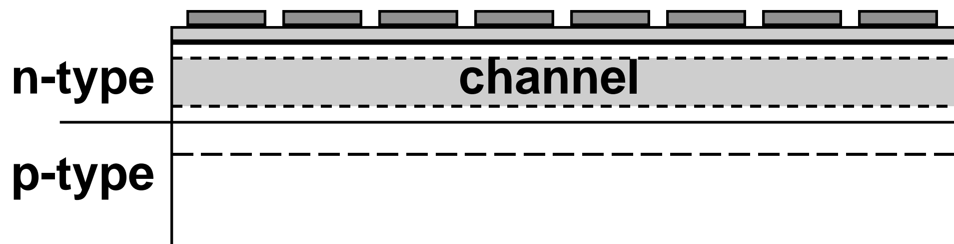
- **The time constant for trapping << time constant for release**
  - » t_{trap} 10^{-9}s (depends on electron concentration
  - » $t_{release}$ $10^{-11} – 10^{-3}$s (depends on trap depth)

Reducing Charge Trapping

- **One way to reduce the effects of charge trapping is to keep the traps permanently filled**
  - » so-called “fat zero”
  - » giving $Q_{total} = Q_{fz} + Q_{signal}$
  - » Q_{fz} 20% of full-well capacity
- **This works well, but has the disadvantage of reducing the dynamic range**
  - » because some of the well is always filled
- **Modern processing technology is quite good at minimising surface states**
  - » but there are always some left
- **So the best way of reducing their effect is to**
  - » remove the interface
  - » or at least move the charge storage away from the interface
- **The result is known as a <u>buried channel CCD</u>**

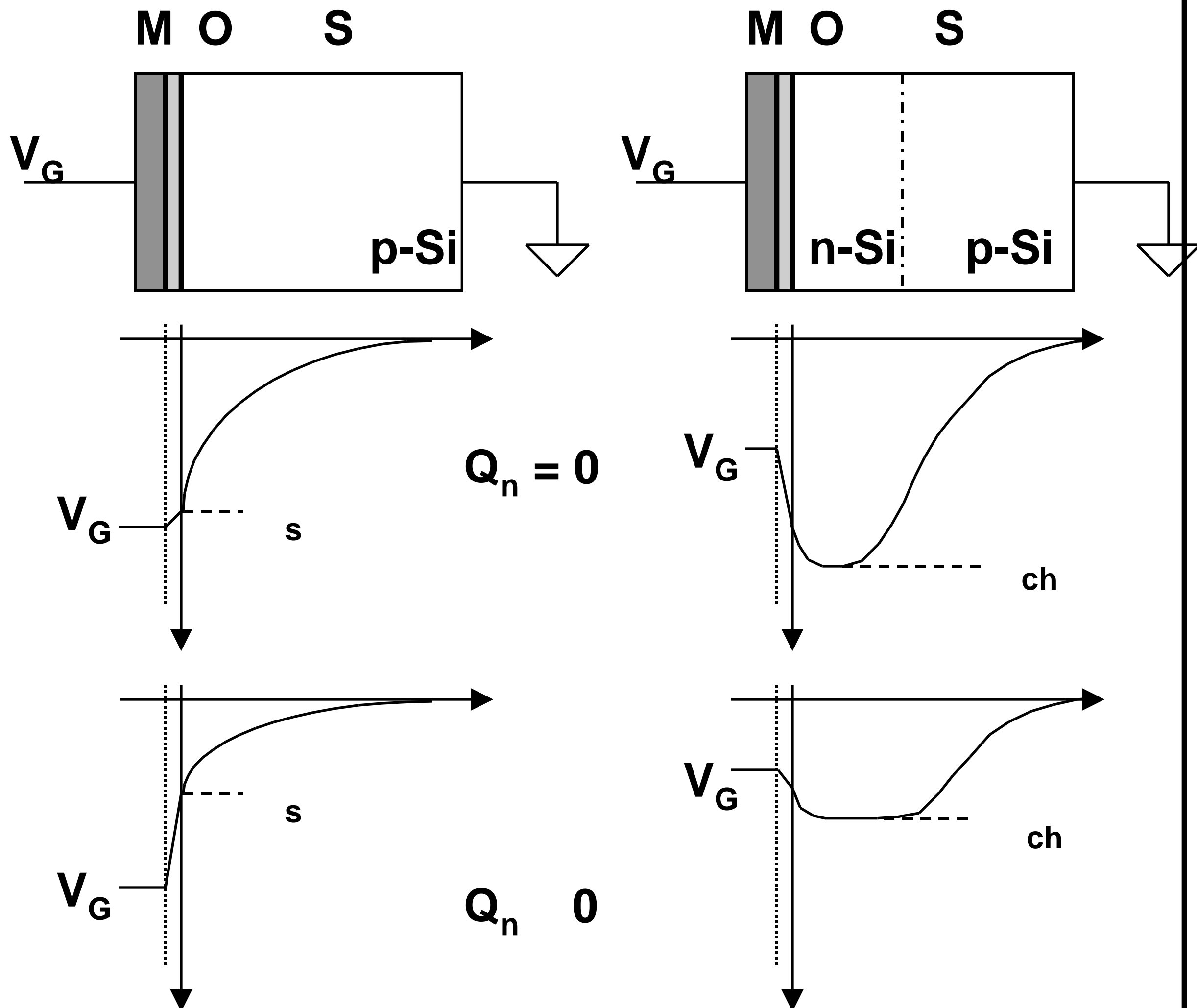
Buried Channels

- **The surface states affect**
  - » charge transfer efficiency
  - » dark current (more easily generated when there are mid-gap states)
  - » noise
- **So buried channel devices use extra implants to move the “active” area of the CCD away from the Si-SiO_2 interface**



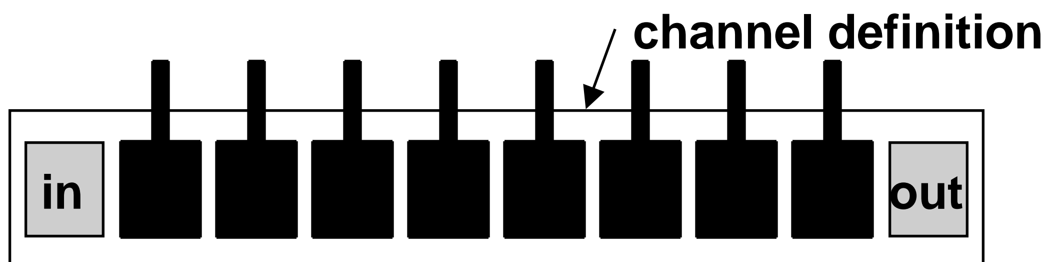
- **The doping is such that the n-type is fully depleted**
  - » the exposed N_d^+ ions enhance the positive potential from the gate
  - » and creates a potential minimum that is away from the semiconductor surface
  - » typically the n-type is 0.3μm thick & N_d 3.10^{16} cm^{-3}

- **The potentials for empty and partially full wells are as follows**



- **As the well fills, the channel moves closer to the surface**
    - » and eventually the charge packet interacts with the interface, as before

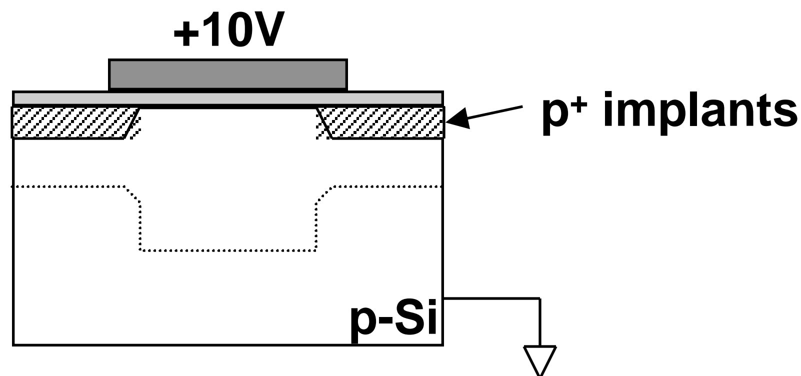
- **In addition to the reduction of charge trapping, BCCDs have another advantage**
  - » fields increase more with depth below the surface
- **Hence, the charge transfer is both more complete and faster**
  - » provided you have enough voltage on the gates to achieve the greater depletion depth
- **However, the main drawback of the buried channel approach is that the total charge-handling capability is reduced**
  - » because the “capacitor” on which the charge is stored is smaller, since the “plates” are further apart
  - » this difference may be about a factor of 3
- **While we have now covered some of the basic background of the CCD, two more additions are needed**
  - » something to stop the charge spilling sideways out of the CCD



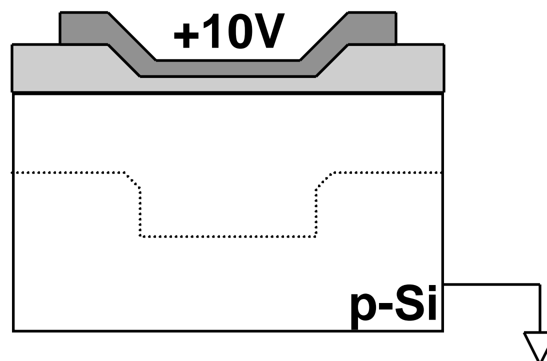
  - » something to handle charge when the well overflows

Channel Definition

- **There are two common methods for channel definition**
- **Channel-stop implants**
  - » the threshold voltage for channel formation is increased beyond the gate voltage by the p+ implants
  - » so the channel only forms in the region in-between

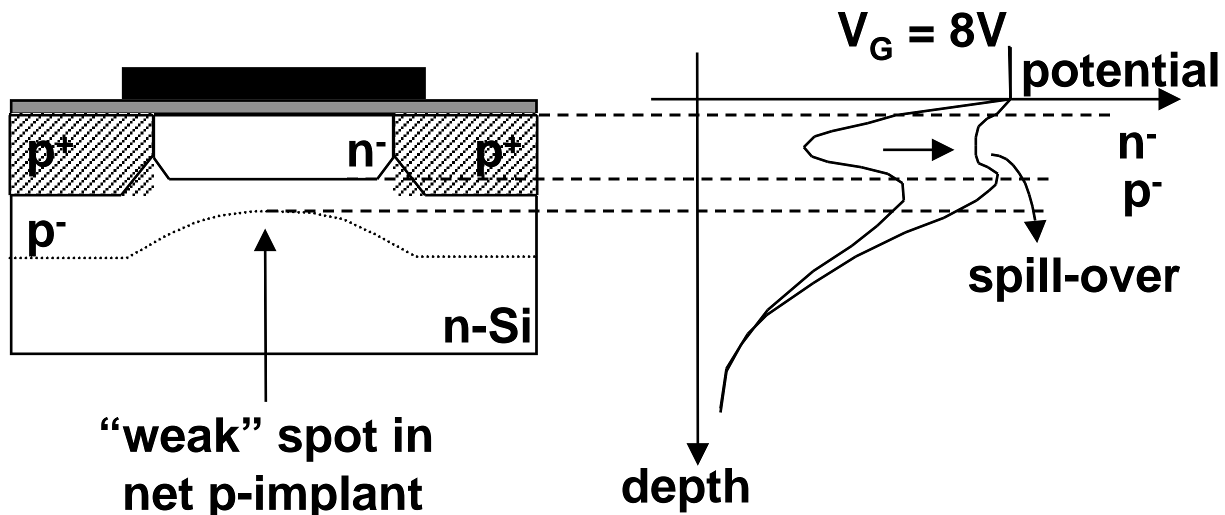


- **Stepped oxide isolation**
  - » the gates are moved further away from the substrate, thereby reducing the field underneath
  - » called LOCOS (LOCal Oxidation of Silicon)



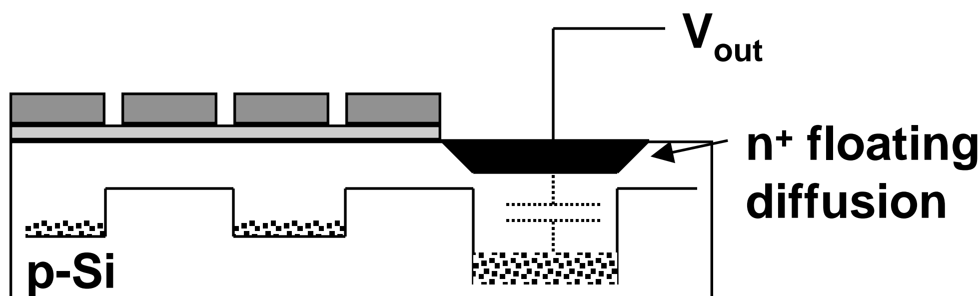
Vertical Anti-Blooming

- **Remember that one of the image artifacts – blooming – was caused by charge from one brightly illuminated pixel spilling into neighbouring pixels?**
- **Vertical antiblooming is a compact method by which to drain away excess photo-generated carriers**
  - » in cross section, the device has the p^+ channel stops
  - » and the n^- buried channel layer
  - » a non-uniform p-implant, leading to a “weak” point at which the spill-over will occur



Charge Readout

- **The clever part about using charge as the signal (rather than voltage or current) is that we can convert charge to voltage with a high degree of sensitivity**
  - » by using a capacitor; $V = Q/C$
- **So if we make C small enough, we get a large voltage for a small charge**
  - » typically 10µV per electron
  - » so a full well of 10^5 electrons gives an output of 1V



- **The corresponding capacitance is about 16fF**
  - » so the diffusion must be small and lightly doped
- **So now the tactic of waiting longer to integrate more charge on the pixel makes sense**
  - » we pass on discretised packets of charge, rather than a continuous current
  - » because the conversion method is more sensitive

Fabrication

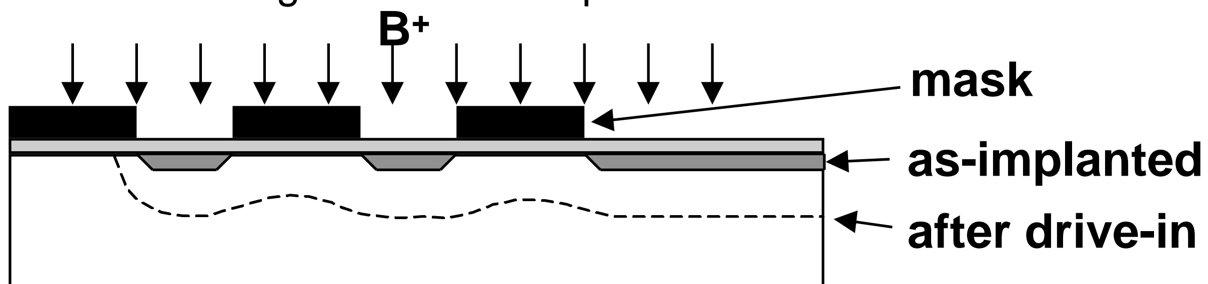
- **Having seen how a CCD works, we can now look at what fabrication processes must be optimised**
- **We will find that a good CCD demands a process that is substantially different from other fabrication technologies, notably CMOS**
  - » and the trends of “mainstream” technologies are exactly to opposite to those required for CCDs
  - » indeed, some trends are also bad for CMOS imagers too – see later!
- **The main issue is that CCDs are, by today’s standards, macroscopic devices**
  - » and need to be that way for effective imaging & charge transfer
- **While CMOS technology, with its standard libraries and wide availability is getting ever more microscopic**
  - » for higher speed
  - » and lower power consumption
- **CCD fabrication is complex with typically 15 - 25 masks**
  - » so we will only look at a the basic features

Requirements

- **We can already summarise some of main conditions**
- **Double (or more) poly-Si process**
  - » for overlapping gates
- **Deep, complex implants which define**
  - » buried channel and p-well (with VAB)
  - » channel stops
- **Relatively high operating voltages**
  - » to get a good potential well in the buried layer
  - » typically 10 - 20V
- **The serial nature of the CCD means that, conventionally, all of the video data passes through a single output node**
  - » this is good because it reduces errors due to component mismatch
  - » but the subsequent electronics has to able to cope with the video-rate data
  - » which is tough without speed-optimised devices
- **To reduce this problem some CCDs are sub-divided and have several outputs**

p-Well

- **The p-well is formed from implanted B ions**
  - » ~100keV & ~10^{12} cm^{-3}
- **Under the photo-sensitive elements, the location of the well "weak" point is defined by masking out the implant**
  - » a thin SiO_2 layer is used to protect the surface from damage due to the implantation



- **Implantation is followed by "drive in"**
  - » the wafer is heated to ~1100°C for 10 hours
  - » the dopants diffuse downwards and laterally
  - » $L_{lateral}$ $0.75L_{downwards}$
  - » this fills in the gaps between the implants to give the "weak" point required for VAB
- **The final depth of the p-well is ~2.5µm at the shallow point and 3.0µm elsewhere**

Channel Stop Implant

- **The p^+ channel-stop regions are again formed using ion implantation**
  - » B^+ ions at 50keV and 2×10^{13} cm^{-3}
- **This implant is driven in during the high temperature cycle (>1000°C) used next to grow the gate oxide**
  - » to a final depth of about 1μm
- **A trade-off here is that driving the p^+ implant deep enough also causes it to spread sideways**
  - » taking up valuable space between the rows of pixels
- **An important fact to note is that there are several high temperature process steps, each requiring temperatures in excess of 1000°C, e.g.**
  - » p-well drive in
  - » channel drive-in
  - » gate oxide
  - » inter-poly oxides between gates
- **So the final depth of the implants is a function of the cumulative effects of all these steps**

Gate Oxide Thickness

- **The oxide layer that isolates the gates from the channel is grown using the same high-temperature step that drives in the channel stop**
- **The original protective SiO_2 layer is removed and the wafer cleaned**
  - » thermal oxide offers the best Si – SiO_2 interface
- **A typical gate oxide is 80nm thick**
- **Compared with values for modern CMOS processes (< 10nm), this is very thick**
  - » and is needed because of the higher CCD operating voltages
  - » 10V as opposed to 3.3V (or less)
- **Later fabrication stages include**
  - » deposition and patterning of several poly-Si layers and inter-poly dielectrics
  - » (this gets tricky because of the surface topography)
  - » metal layers and contact vias
  - » n^+-implants to make source/drain regions at the CCD input and output
  - » colour filters and/or microlenses