Part II:
Fabrication Technology and Pixel Design

Introduction

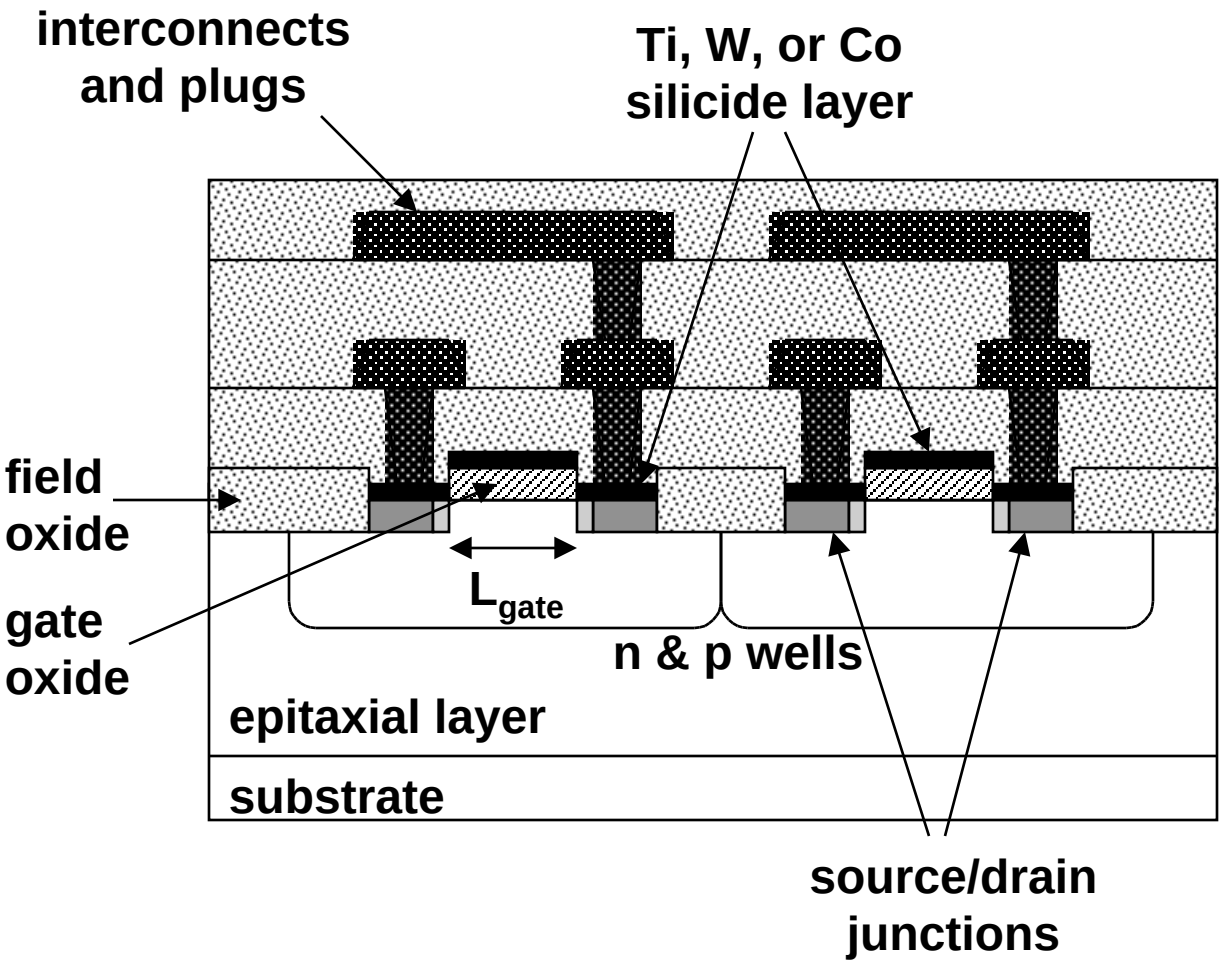
- **In this section we will take the ideas of optical detection and examine how they can be applied to practical optical detectors**
- **We also need to know how the fabrication technology influences the performance of the sensors**
- **So we will first look briefly at CMOS technology, and then dwell longer on how the future development of CMOS will affect image sensors**
- **In the second half of the section, we will discuss the four basic types of CMOS pixels**
  - » passive pixel photodiode
  - » linear active pixel photodiode
  - » logarithmic active photodiode
  - » photogate active pixel

Fabrication of CMOS Imagers

- **The first part of the idea of using “standard” CMOS technology for imagers is to use a widespread, accessible process**
  - » with well-developed design tools
  - » standard design libraries
  - » fast turn-around time
- **The second part is that fully integrated camera systems can be built on a single chip, featuring**
  - » low power consumption (low voltage operation)
  - » small, robust, and inexpensive
  - » integrated clocking and addressing
  - » focal-plane image processing
  - » A-D conversion, signal encoding
- **We will find that, while the second part is becoming true, there may be some problems with the first part**
- **Here, we examine the trends of CMOS technology and their implications for fabricating imagers**
  - » we will also compare briefly CCD and CMOS technologies, and consider the hybrid CCD/CMOS

Features of Sub-micron CMOS Technology

- In the following few pages, we will examine the evolution of CMOS technology
- A simplified cross section through a sub-micron CMOS process is shown below to illustrate the relevant features



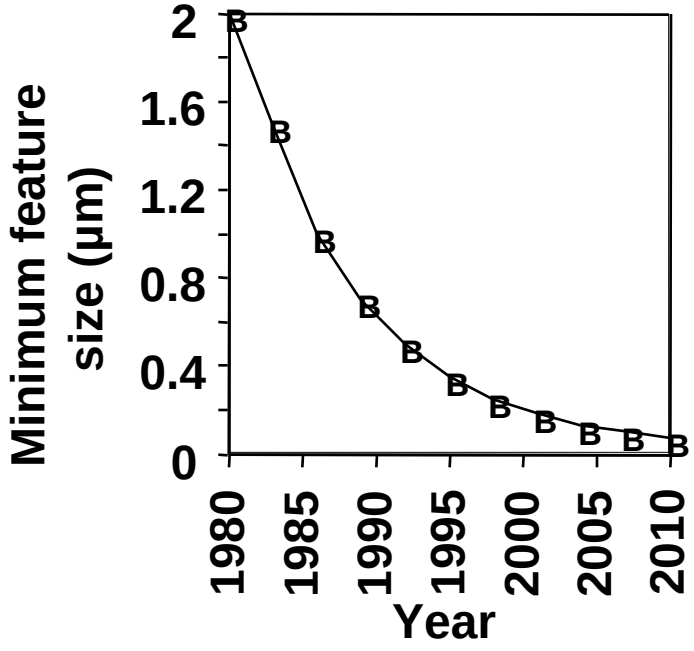
Effects of Technology Scaling

- **One of the "selling points" for the surge of interest in CMOS imagers has been the attraction of using standard processing to**
  - » reduce development costs
  - » reduce fabrication costs
  - » reduce dependence on a single supplier
- **However, the question was naturally asked about how the rapid development of these "standard" processes would influence the imager performance**
- **The following pages are based on the 1994 Semiconductor Industry Association roadmap**
  - » the updated 1997 version applies even more so!
- **Each aspect of scaling will be considered individually, along with the potential impact on CMOS imagers**
  - » the seminal work on the subject is by Wong, from IBM (see references)

Feature Size

- **A new generation of CMOS devices is developed every three years, or less**
  - » device dimensions are less than 0.7 times those of the previous generation
  - » 0.25µm technology is in production
- **This is driven by the desire for**
  - » lower power consumption
  - » higher speeds
  - » increased functionality

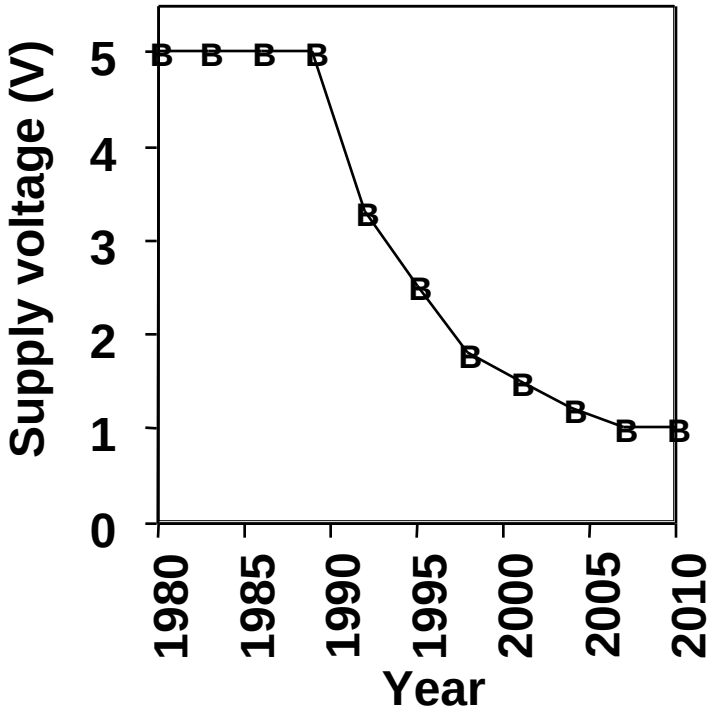
good for integrated cameras too!



- **Additional impact on CMOS imagers**
  - » improved fill factor
  - » improved conversion efficiencies

Lower V_{DD}

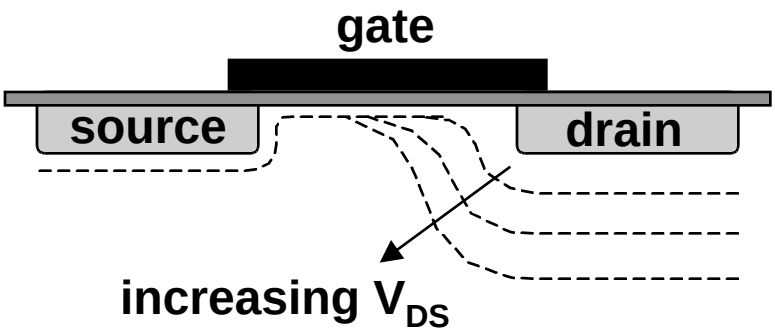
- **Partly forced by reduced dimensions**
  - » because electric fields cannot be too high
  - » e.g. hot carrier effects & tunneling
- **Partly for lower power consumption (P V_{DD}^2)**
- **The curve below clearly shows the trend towards $V_{DD} \approx 1V$**



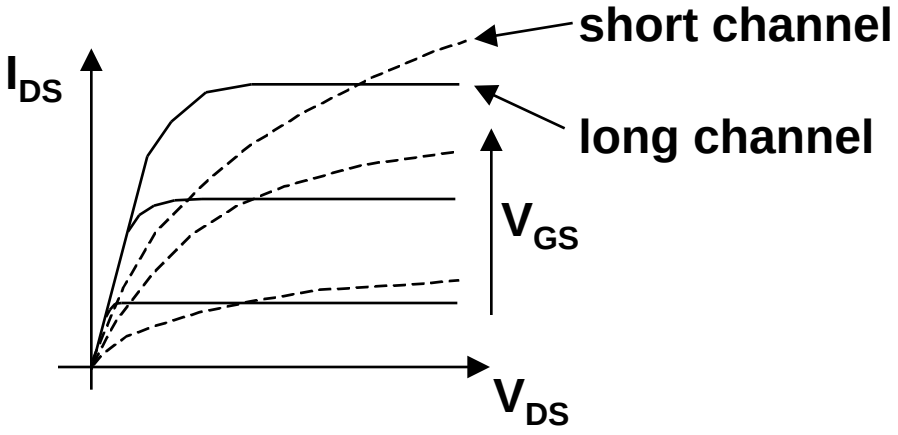
- **Impact on CMOS imagers**
  - » reduced analog voltage swing, $V_{DD} - V_T$
  - » hence, reduced dynamic range
  - » analog signal processing becomes difficult

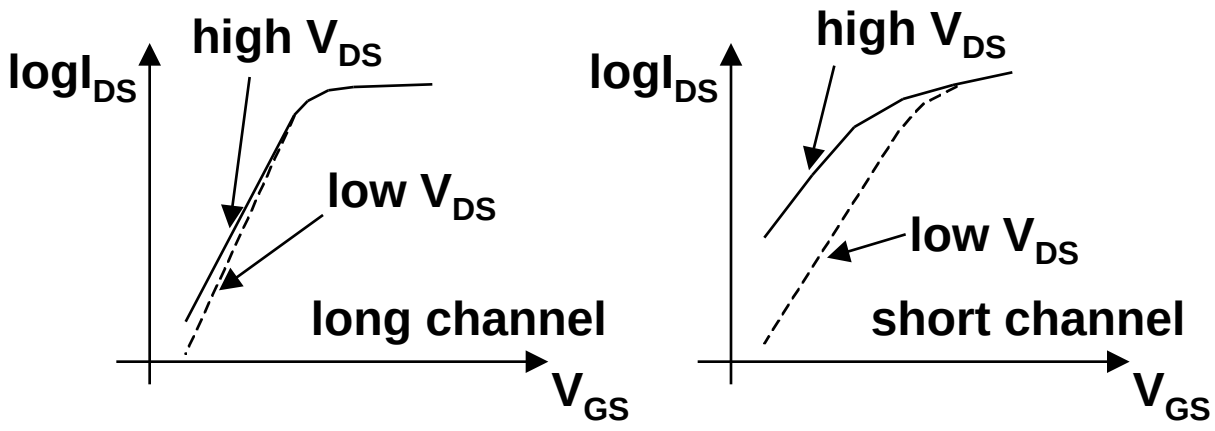
Brews' Rule

- **When the channel lengths of MOSFETs become too short, so-called short-channel effects become apparent**
- **The main effect of this scaling is to reduce the charge under the gate**
  - » which ideally is a function just of the gate potential
  - » but changes due to the depletion width at the drain, and hence with V_{DS}



- **Short- and long-channel effects can be summarised as follows**





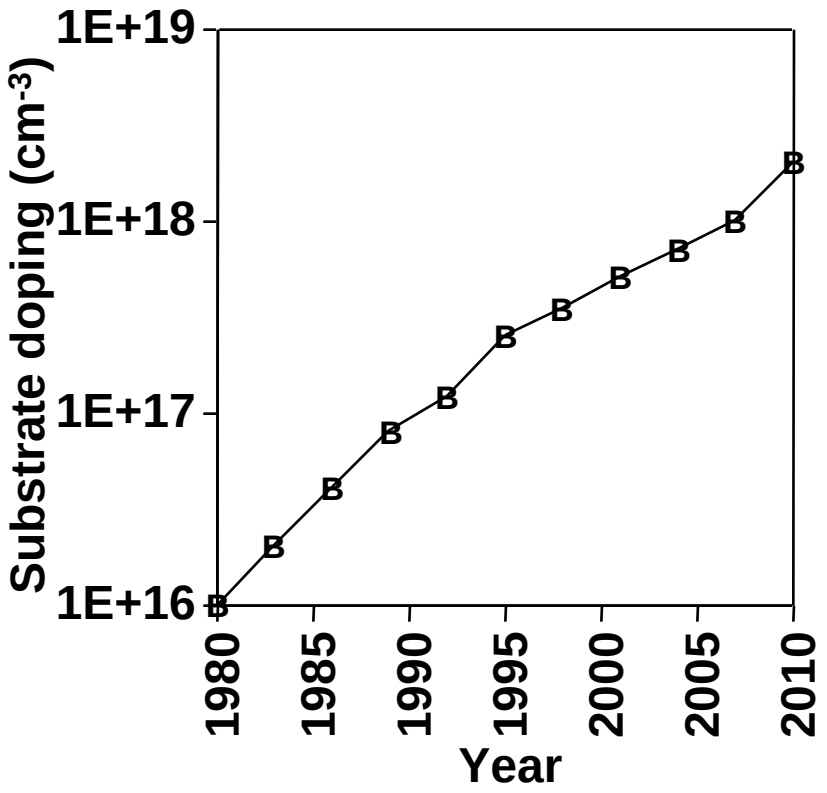
- **A rule of thumb for determining the minimum acceptable device length has been developed by Brews**

$$L_{min} \approx 0.4\left[x_j t_{ox}\left(W_d + W_s\right)^2\right]^{1/3}$$

- **Where**
  - » x_j is the junction depth in μm
  - » t_{ox} is the oxide thickness in Å
  - » and W_s and W_d are the source and drain depletion widths in μm, respectively
- **Impact of short channel effects on CMOS imagers**
  - » increased off-current of MOSFETs (increases exponentially as V_T is reduced) is a potential issue for some architectures
  - » p-n junction tunnelling current adds to the pixel dark current arising from thermal generation

Substrate Doping

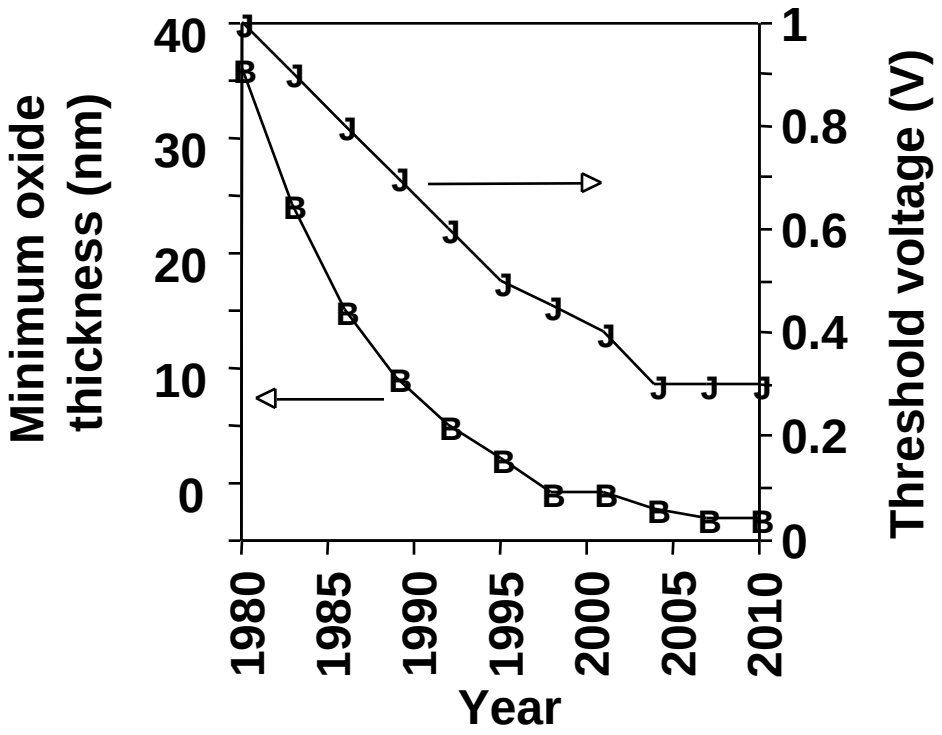
- **$W_{S,D}$ are dependent on the substrate doping of the wafer**
  - » this is increasing over the years in order to minimise short-channel effects



- **Impact on CMOS imagers, due to associated reduction in minority carrier diffusion length, L_n**
  - » good – reduces crosstalk between pixels
  - » bad – reduces effective volume for photo-charge collection

Oxide Thickness

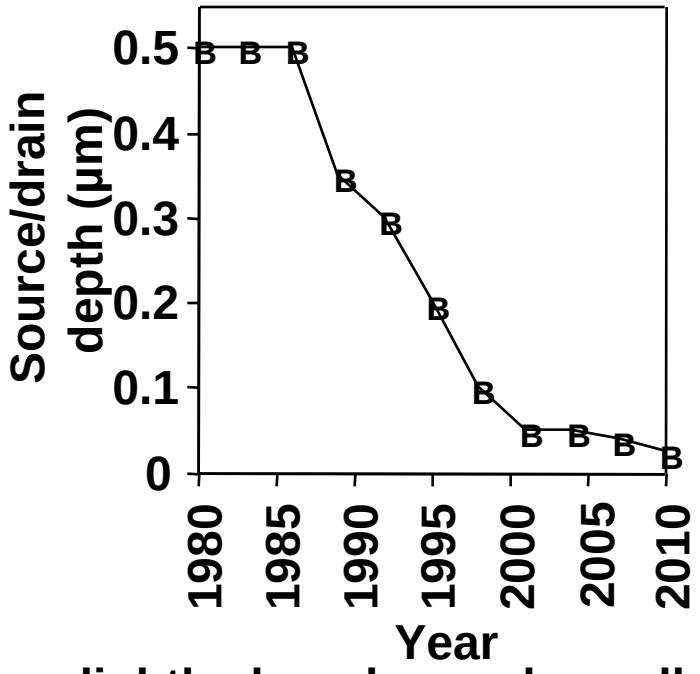
- **As the supply voltage decreases, so too must the threshold voltage**
  - » although this is also affected by substrate doping
- **V_T is dependent on $1/C_{ox}$, and therefore t_{ox} must be reduced, since $C_{ox} = \varepsilon_{Si}/t_{ox}$**



- **Impact on CMOS imagers**
  - » reduced voltage swing, as before, since V_{DD} scales faster than V_T (see later for plot of trend in $V_{DD} - V_T$)
  - » gate tunnelling current potentially important for some MOS capacitor devices

Source/Drain Junction Depth

- **Source and drain junction depths are important in determining the influence of the drain depletion region on the MOSFET characteristics**
  - » as indicated in Brews' rule



- **More lightly doped n- and p-wells may be a few times deeper than the junction depths**
  - » so, ~ 0.5μm at the moment
- **Impact on CMOS imagers**
  - » reduces the effective volume for collecting photo-charge, hence reduced quantum efficiencies
  - » possible increase in surface effects

New materials

- **One major change that has been made in the materially-conservative semiconductor industry is the introduction of silicide layers**
  - » to reduce contact and sheet resistances of source/drain regions and gates, respectively
  - » usually WSi_2, $TiSi_2$, $CoSi_2$
- **This is important for imagers because silicides are relatively opaque to visible light**
- **At the 0.5μm technology level, silicide layers can be optionally masked out**
  - » but it is not clear whether this will continue to be the case in future technologies
- **Mendis has reported that a pixel's sensitivity is reduced to 20% of its former value in the presence of the silicide layer**
  - » which is consistent with the silicide transmission spectrum

Conclusions

- **Wong's conclusions may be summarised as follows**
  - » full integration offered by CMOS devices is still advantageous
  - » sub-0.5μm technology will not be optimal for imaging without some process changes
  - » other costs (packaging, testing) are more important than the extra costs incurred by using a slightly non-standard process
- **While Wong's conclusions may be technically correct, it is still not clear what influence technology scaling will actually have**
  - » cheaper and wider access to older technologies may remain more attractive
  - » process tweaks do not just raise costs, but also reduce second sourcing options and portability
  - » even if advanced technologies are used, the system design may mitigate many disadvantages without the need for tweaking
- **In the end, the balance depends on the application**
  - » and it is likely that a continuum of techniques will develop between pure CCD and pure CMOS

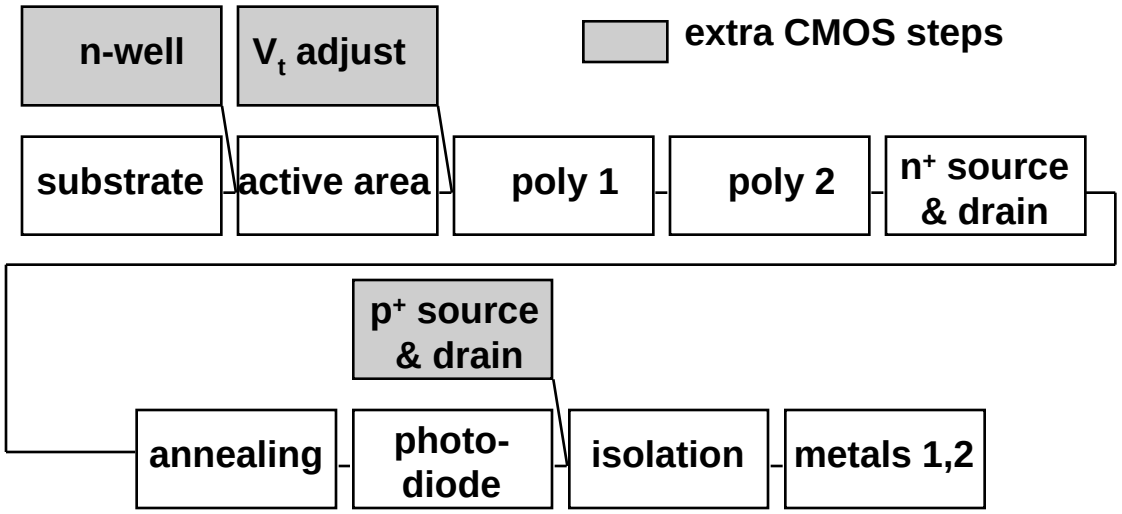
Comparison of CMOS & CCD Technologies

- **We can write down broad requirements for each technology**
- **CCD**
  - » gate oxide thickness ≈ 800Å
  - » p-well depth > 2.5µm
  - » channel stop depth ≈ 1µm
  - » channel depth ≈ 0.8µm
  - » typical operating voltage ≥ 10V
  - » several poly-Si and inter-poly dielectrics needed
- **CMOS**
  - » gate oxide thickness ≈ 50Å
  - » well depths ~ 0.5µm
  - » source/drain implants ≈ 0.1µm
  - » operating voltage ≤ 3.3V
  - » digital process has 1 poly, analog has 2 polys
- **A comparison of these figures makes clear why it is difficult to integrate the two technologies**
  - » essentially, a full-featured combination would require almost all the stages from both processes
  - » which means maybe > 30 masks

Combined CMOS/CCD

- **To date, the reduced yield and increased costs has not made a combined CMOS/CCD process viable**
- **The combined process is neither standard CMOS nor standard CCD, and so requires extensive development expenses**
  - » and the frequent result is that neither part will work particularly well
- **Several processes have been reported which claim to preserve the quality of each technology**
- **Suni Imaging Microsystems are advertising a hybrid process which has**
  - » only “3 or 4” more masks than standard CMOS
  - » 5V operation
  - » and works by separating out CCD and CMOS regions on the chip
  - » CCDs can run satisfactorily at 5V provided their area is enough to ensure a reasonable full well capacity
  - » for high resolution – small pixel area – higher voltages are generally required to achieve the full well, so some compromise must have been made here

- **The alternate approach is to start with a CCD process and add in extra process modules**
  - » e.g. that reported by Eastman-Kodak
  - » extra CMOS steps added



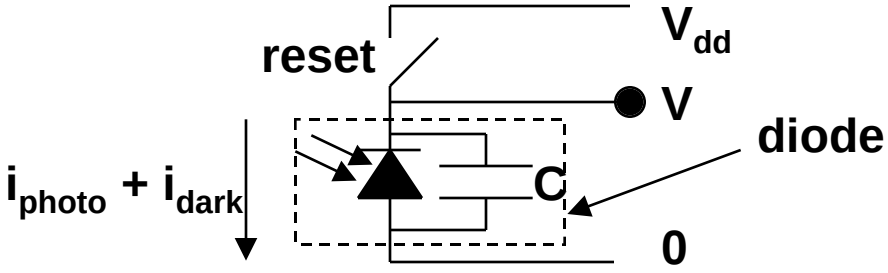
- **Such a process required 4 additional masks and 3 extra implants**
  - » a BiCMOS process is also demonstrated, with 3 additional masks and 3 implants for a NPN transistor
- **Despite the demonstrated feasibility of CMOS/CCD hybrids, the idea has not yet taken off**
  - » possibly because few places have access to both sets of fabrication facilities and design experience

CMOS Photodiode Pixels

- **We have already seen something about how we might build pixels using CMOS technology**
- **Now we will look in more detail at the different designs of pixels that have been fabricated using CMOS**
- **Although there is one dominant sensor type – the photodiode – there are several possible implementations**
- **And there are additional topologies which draw on CCD ideas**
- **Here, we will not dwell greatly on either the rest of the in-pixel circuitry or on the support circuits**
  - » these will be the topic of a future section
- **In passing, we will mention some of the sources of noise in the imaging arrays**
  - » these too will be drawn together later

“Photon Flux Integrating Mode”

- **The operation of a photodiode in the “charge integration” mode discussed earlier is not recent**
  - » it was proposed in 1967 by Gene Weckler
- **In the original proposal, the circuit was presented much as we did before**



  - » although Weckler also demonstrated that a MOSFET could serve adequately as the switch
- **We can follow a simple analysis for the output voltage of the diode as a function of time, after the diode has been reset**
- **Here, we note that the current in the capacitor must be equal and opposite to the photocurrent**
  - » because the diode is isolated
  - » and we will ignore the dark current

- **Hence**

$$C(V)\frac{dV(t)}{dt} = -i_{photo}$$

- **For a n^+p diode, the capacitance is**

$$C_j(V) = \frac{A}{2}\left[\frac{2q\varepsilon_{Si}N_A}{V(t)}\right]^{1/2}$$

  - where A is the diode area, and N_A is the acceptor concentration in the substrate

- **So we find**

$$\frac{A}{2}\left(2q\varepsilon_{Si}N_A\right)^{1/2}\left[2\sqrt{V}\right]_{V_{reset}+V_0}^{V(t)+V_0} = -i_{photo}t$$

  - where V_0 is the diode built in voltage, and V_{reset} is the reset reverse bias

- **And thus**

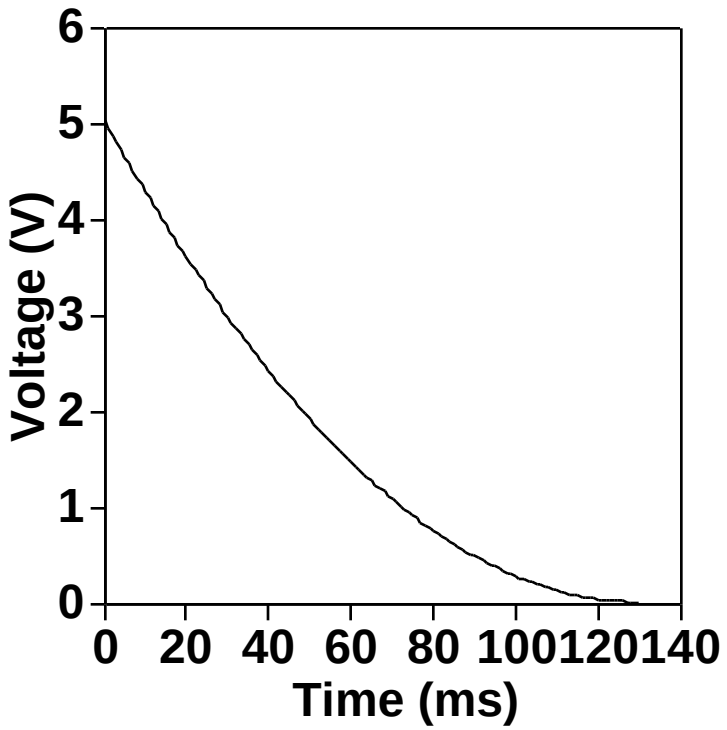
$$V(t) = \left[V_{reset}^{1/2} - \frac{i_{photo}t}{A\left(2q\varepsilon_{Si}N_A\right)^{1/2}}\right]^2$$

- **While this expression includes a term in A, the diode area, this cancels out because**

$$i_{photo} \quad I_0 A$$

  - where I_0 is the incident flux of photons

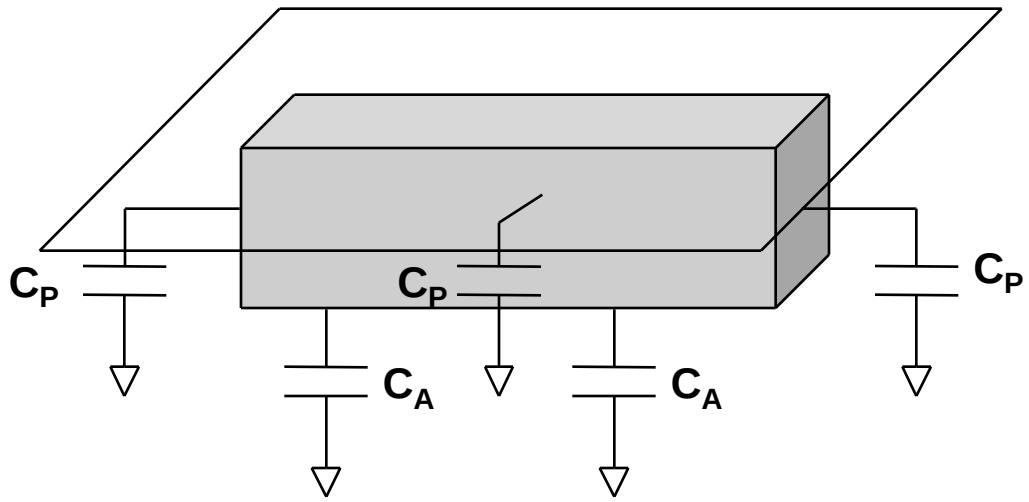
- **So the collected voltage is independent of the diode area for a given photon flux**
  - » if we think of V = Q(A)/C(A), then both Q and C are proportional to area so the voltage is unchanged
- **If we calculate V(t) as a function of time for**
  - » A = $(10\mu m)^2$, V_{reset} = 5V, $N_A = 10^{16}$ cm^{-3} , and i_{photo} = 1pA (small), we find the following curve



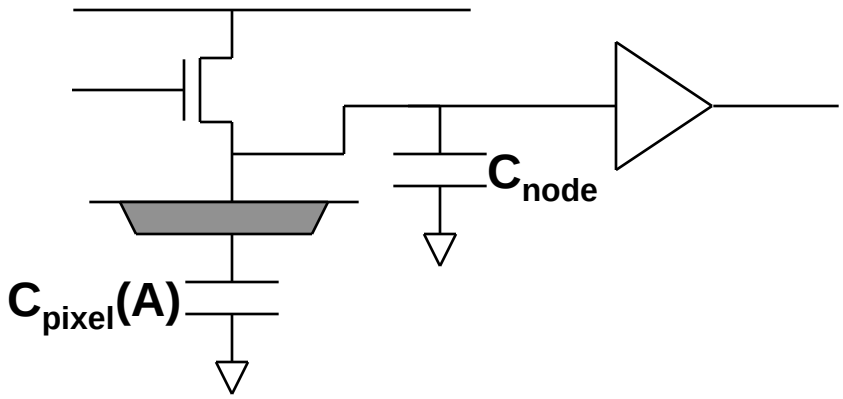
- **The voltage drop is almost linear for short times**
  - » which is what we want!
  - » remember this does not include dark current

Fill Factor

- **So why are we worried about the fraction of the pixel that is light-sensitive – the "fill factor" – if the area cancels out?**
- **This is because the foregoing analysis is only part of the story**
  - » capacitance does not come just from the pixel area
  - » and we must consider sources of capacitance external to the pixel
  - » and there are other unwanted sources of charge
- **Firstly, capacitance arises both from the "floor" (the area capacitance) of the implanted region and from the "wall" (the periphery)**



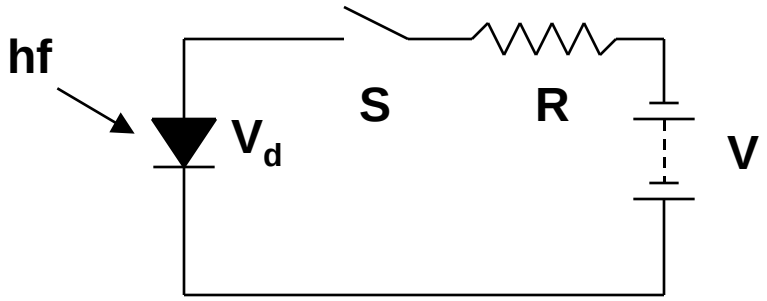
- **For a 0.5μm process, the capacitances at zero bias are**
  - » $C_{ja} = 4.7 \times 10^{-4}$ F/m^2
  - » $C_{jp} = 3.2 \times 10^{-10}$ F/m
- **For a (30μm)² pixel, the periphery represents 0.08 of the total capacitance**
  - » but this rises to 0.3 for a (7μm)^2 pixel
- **Alternatively, the area has scaled by 0.05 from (30μm)² to (7μm)²**
  - » but the capacitance has only scaled by 0.07
- **Thus the smaller pixel generates less voltage than does the larger one**
  - » because i_{photo}/C_{total} has scaled by 0.05/0.07 = 0.7
- **Secondly, the photodiode is connected to the outside world**
  - » either to the column bus or to an in-pixel voltage buffer



- **Hence, there is a fixed capacitance**
  - » i.e. not dependent on the pixel area
  - » so $V_{out} = Q(A)/[C_{pixel}(A) + C_{node}]$
  - » which falls as A decreases
- **Thirdly, there will be sources of unwanted charge that are non-linearly dependent on pixel area**
  - » e.g. dark current comes from both area and periphery
  - » and/or “reset” noise
  - » so $V_{out} = [Q(A) + Q_{noise}]/C_{pixel}(A)$
  - » therefore as A falls, the signal-to-noise ratio falls
- **Fill factor is particularly important for CCDs because the sensing capacitance is external to the pixel**
  - » so the more charge you collect during the integration time – i.e. the larger the photosensitive area – the better
- **A larger photosensitive area also gives a larger full well capacity**
  - » which should give a larger dynamic range
  - » provided the limiting factor on the minimum resolvable signal does not depend on pixel area
  - » usually, it is later elements that limit the dynamic range

Passive Pixel Sensors (PPS)

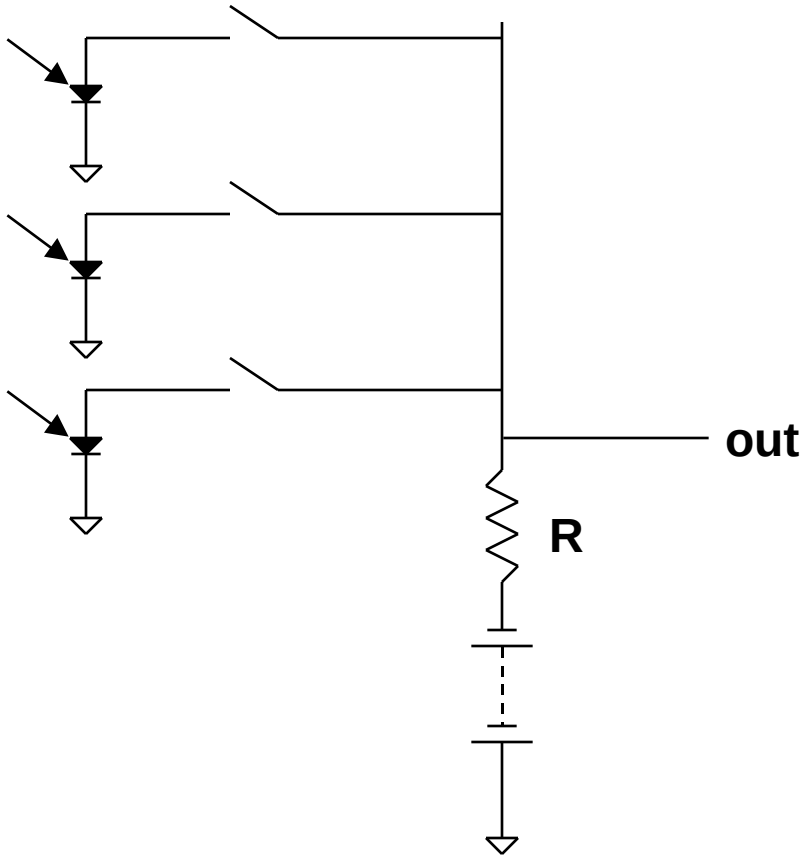
- **Weckler's method for reading out the integrated charge was to measure the voltage across a load resistor required to reset the pixel**



  - » switch, S, is closed to reset the pixel to a reverse bias of V
  - » for a period of t_{int}, S is opened, allowing the photodiode to discharge at a rate approximately proportional to the incident illumination
  - » when S is closed again, the total charge that must flow through R to reset the pixel is equal to that "lost" during the integration period
  - » and the signal across R is a measure of the voltage on the photodiode after the integration time

- **Weckler also reported the first picture from a photodiode array (a 200-element linear array)**
  - » he named it a reticon and founded the company of the same name (now EG&G Reticon)
  - » and he holds the first patent on photodiode arrays

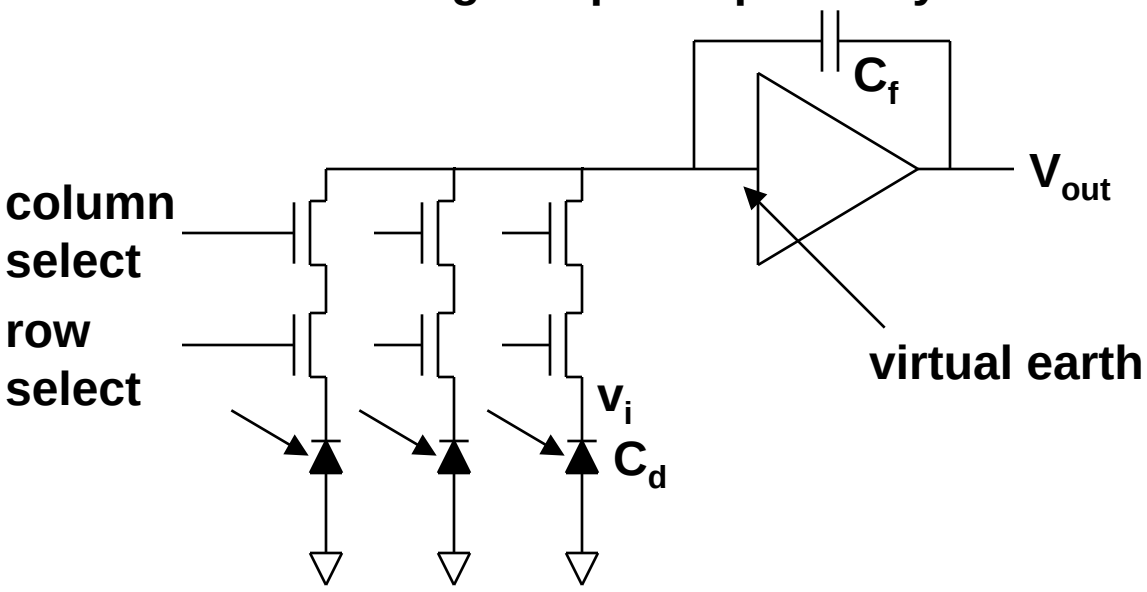
- **To integrate this into an array, the suggestion was to use a single load resistance at the bottom of a column of pixels**



- **One of the disadvantages of this readout technique (especially for large arrays) was the time required to reset the diode fully through the resistor**
  - » incomplete reset reduces the dynamic range of the sensor
- **Hence, readout via a charge amplifier was suggested**

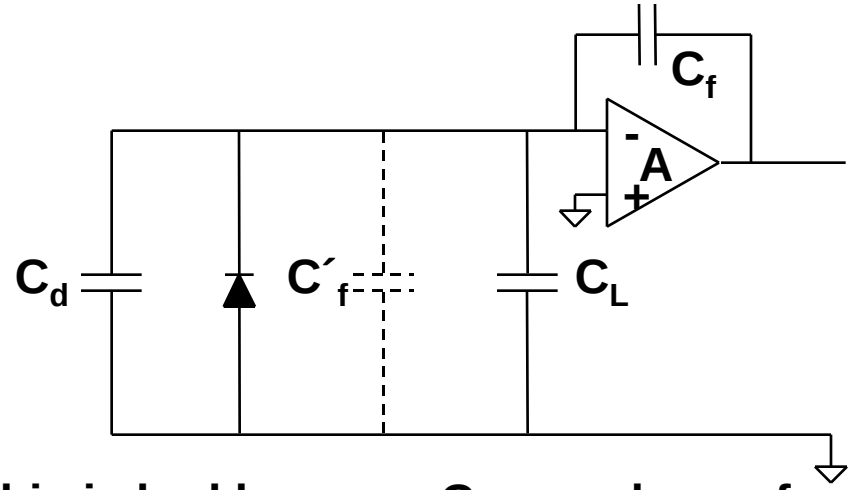
Charge Amplifier

- **An alternative to the resistor readout scheme is to supply and measure the reset charge using a charge amplifier**
- **As proposed, for example by Noble (1968), there would be one charge amplifier per array**



- **In the ideal case, the virtual earth of the amplifier would supply the current needed to recharge the diode**
  - » once the appropriate addressing transistors are turned on
- **This current would be integrated and converted to a voltage**
  - » $V_{out} = v_i.C_d/C_f$

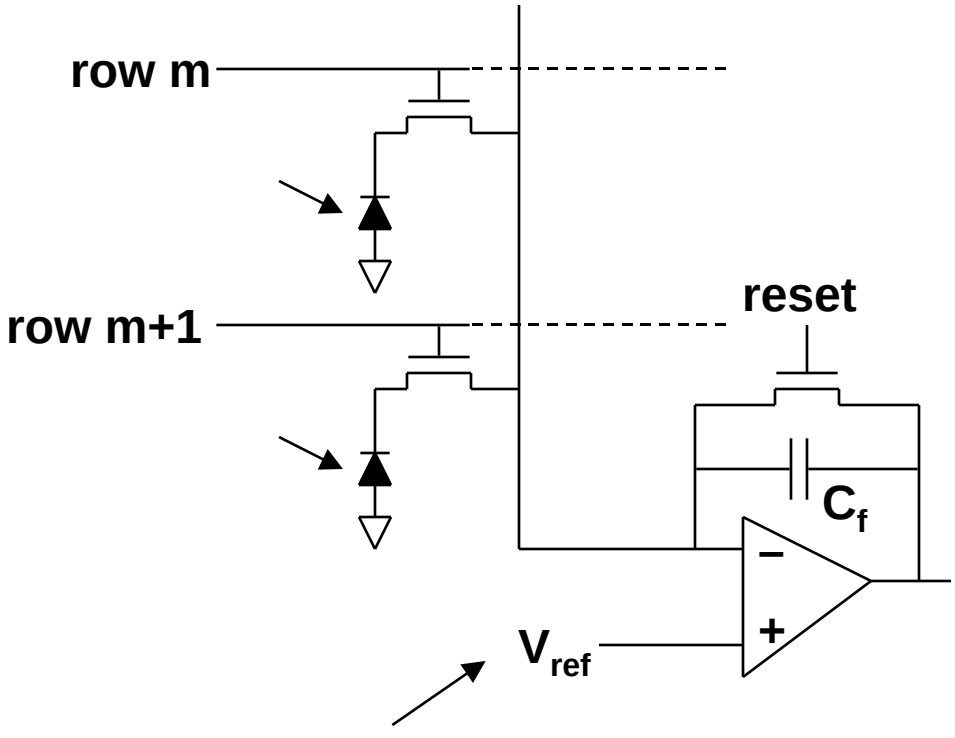
- **This charge is stored on C_f after the column or row transistors are turned off**
  - » and the amplifier and the whole line must be reset between pixels by shorting C_f
- **While this approach is simple in principle, it is almost useless in practice**
  - » owing to parasitic capacitances, C_L, of all the data lines, since all diodes are connected to the one input



- **This is bad because C_d can charge from C_L instead of C_f – charge is shared between C_L & C_f**
  - » and so C_f will not record the full charge required to reset the diode
- **The effective value of C_f at the amplifier input is**
  - » $C´_f = (1 + A)C_f$ (from Miller's theorem)
  - » and only $C´_f/(C´_f + C_L)$ of the reset charge comes from the charge amplifier
  - » hence the value of V_{out} can be significantly reduced

Modern Implementation

- **Many research groups and companies have used PPS**
  - » we will consider the pros and cons below
- **The modern implementation reduces the capacitance problem by**
  - » using one charge amplifier for each column in the array
- **And use just one addressing MOSFET**



- **When the address transistor is switched on**
  - » a current flows via the resistance and capacitance of the column bus because of V_{ref} - V_{diode}
  - » this total charge required for this reset is integrated by the capacitor C_f, and output as a voltage
  - » so the final bus and diode voltages are returned to V_{ref} by the charge amplifier
  - » the address FET is turned off, and the voltage across C_f is removed by the reset FET
- **The column bus R & C is still important because they affect**
  - » the speed at which the pixel can be read out
  - » and the noise associated with the readout (see later)
- **Thus the use of PPS these days is limited to small array sizes and slow readout**
  - » typically the “quality” is about 1/10 that of a CCD detector of similar dimensions
  - » and PPS are generally out of fashion
- **Two problems arise from the use of one charge amplifier per column**
  - » differences between amplifiers
  - » reset speed is limited by the maximum size of FETs that can fit into the limited space available in the width of a column

Typical Values

- **A typical 0.5μm process has a metal-1 to substrate capacitance of 50aF/μm²**
  - » leading to the capacitance of a 3μm x 10mm bus of not less than 1.5pF
  - » and there is extra capacitance due to the devices attached to the bus, say 2pF
- **Recall that the (30μm)² pixel capacitance is about 0.15pF**
  - » so about 10% of the bus capacitance
- **A typical value for C_f is 0.2pF**
  - » which gives an effective value of $C'_f \approx 20pF$ at the input to the charge amplifier
- **This means that only ≈ 90% of the charge required to reset the diode comes from the integrating capacitor**
  - » this represents a significant loss of sensitivity

Advantages of PPS

- **Despite the drawbacks in the readout technique of PPS, they have some advantages**
- **The main advantage is that the fill factor is maximised**
  - » because there is only one transistor
- **This allows the pixels to be smaller for a given technology**
  - » which keeps die sizes smaller
  - » and devices cheaper
- **It is also argued that the simplicity also enables a higher yield to be achieved**
  - » which would also keep costs down
  - » but this is less important in these days of high quality fabrication
- **In common with other photodiode-based sensors, the quantum efficiency is high**
  - » because there are as few layers as possible overlaying the device

Hitachi R&D Effort

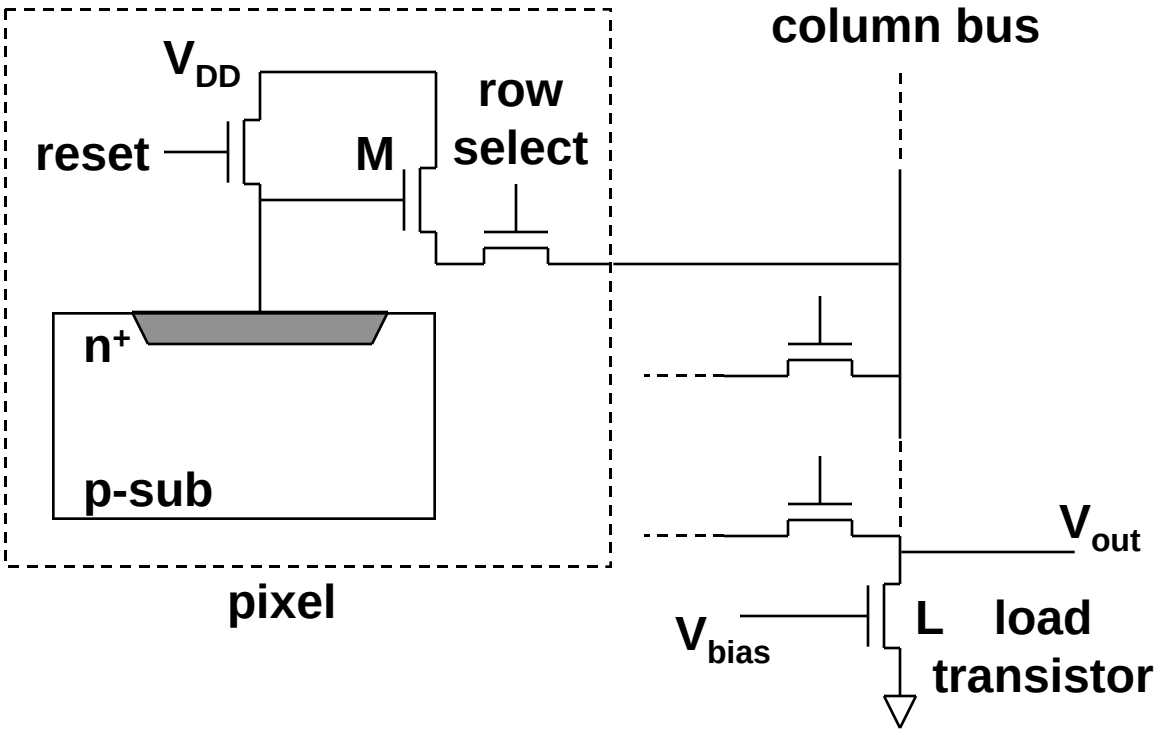
- **One of the few companies to carry out serious R&D into CMOS image sensors in the years between ~1970 and ~1990 was Hitachi Ltd.**
  - » seeking alternatives for colour hand-held video cameras
- **In a series of papers, Hitachi researchers reported essentially complete single-chip colour cameras**
  - » at relatively low 484 x 384 resolutions
  - » but the fabrication technology was 3µm NMOS
  - » this type of integration has only been achieved in commercial products in the last few years
- **These Hitachi sensors were still the passive pixel arrangement**
- **Hitachi abandoned their efforts in the late 1980s**
  - » but they hold several vital patents for active pixels and noise reduction circuitry
  - » these patents are still in force today, so other companies are having to take these into account

Active Pixel Sensors (APS)

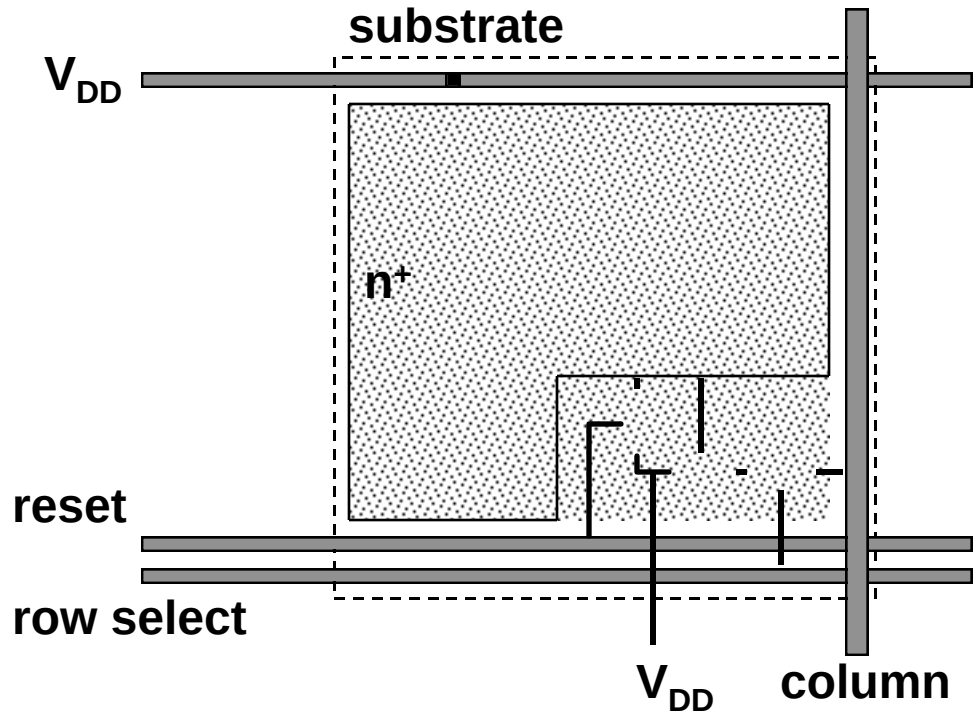
- **In the same 1968 paper, Noble shows the first use of a MOSFET buffer amplifier in the pixel**
  - » this has become known as an active pixel sensor (APS), which Noble also considered to be superior to the PPS
  - » and an improved study and analysis was reported by Chamberlain shortly afterwards
- **In these early devices, variations between the individual diodes and MOSFETs were significant**
  - » variations in diode dark currents and MOSFET threshold voltages
  - » variations in leakage, capacitance etc. in circuitry
- **Overall signal-to-noise ratios were only about 1**
- **It was these variations, due to the immature fabrication technology, that allowed CCDs to gain the dominance that still exists**
  - » CCDs had a smaller fixed pattern noise
  - » and a smaller pixel size because there were no (large) transistors in the pixel
- **Relatively little APS research was carried out for another 10 years, and it took 20 years for major interest to be renewed**

Modern APS

- **With improvements in the CMOS fabrication process brought about by the computer industry, CMOS imagers have again become viable**
  - » these improvements have reduced device-to-device variations to manageable levels
  - » while they are not yet as good as CCDs, the other advantages of CMOS imagers frequently make the performance penalty worthwhile
- **The basic form of APS employs the familiar photodiode, and a readout circuit of three transistors**

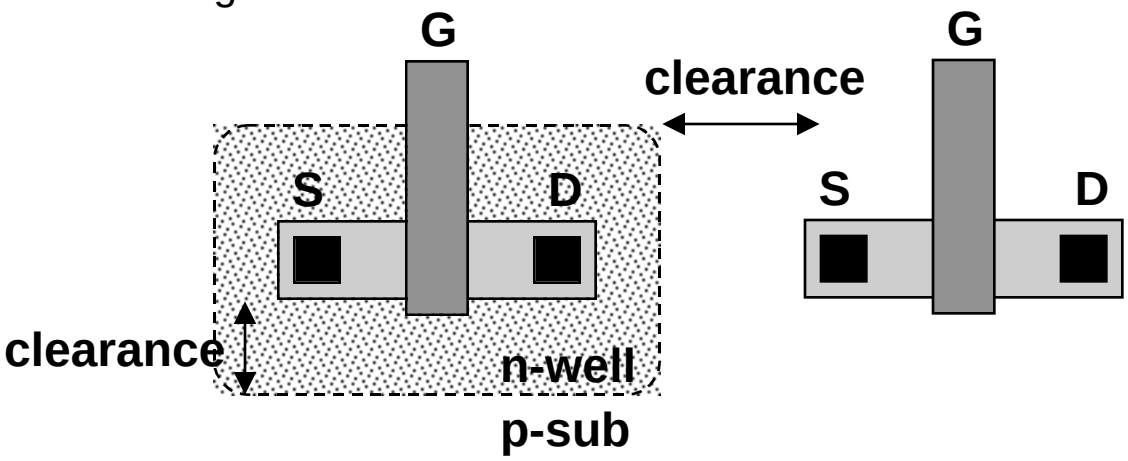


- **Here, the idea is that the photodiode capacitance just includes**
  - » the diode itself
  - » the source of the reset transistor
  - » and the gate of the MOSFET, M
- **M acts as a voltage buffer to drive the output independently of the diode**
- **There is a single load transistor for each column**
  - » this minimises pixel area
  - » minimises pixel-to-pixel variations
  - » and works because only one row of the array is activated at any time
- **A typical pixel layout would look like**



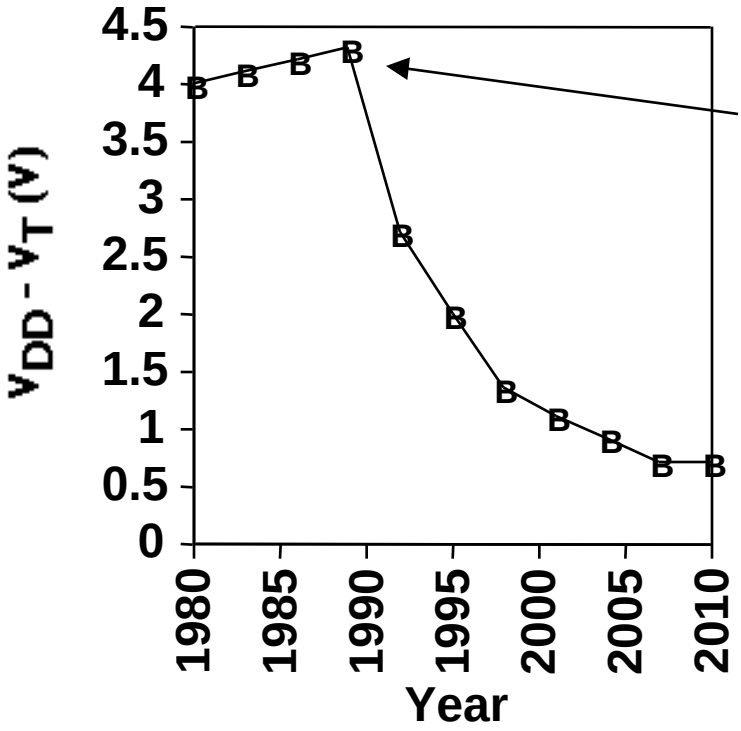
Reset

- **Fabrication usually takes place into a p-type substrate**
  - » and the n^+ source/drain diffusions of the NMOS transistors are used for the photodiode
  - » n-type device wells are needed for PMOS transistors
  - » and there needs to be space both between the devices and the well, and between the well and other things



- **Hence NMOS transistors are most space-efficient because they do not need a separate device well**
  - » which takes up valuable pixel area
  - » and NMOS reset transistors are currently almost universal

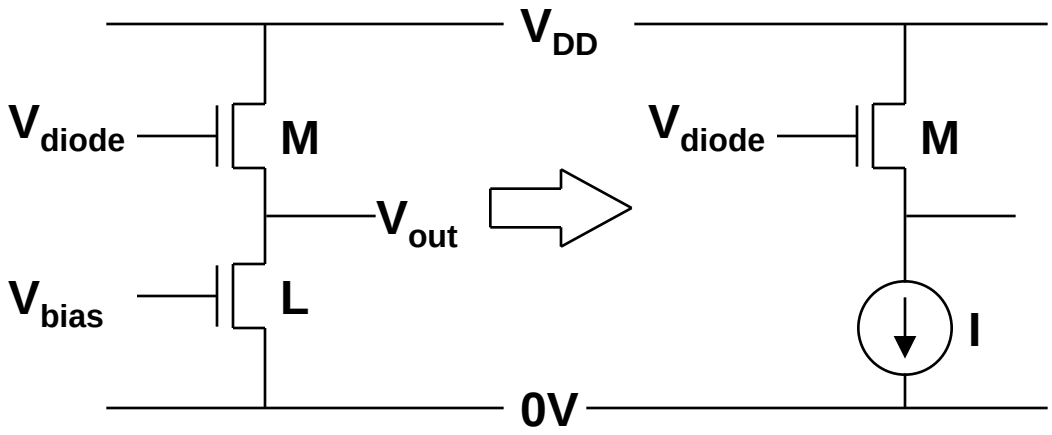
- **However, this has an important drawback**
  - » an NMOS transistor with V_{DD} on both G and D can only get to a source voltage of $V_{DD} - V_T$
  - » before it switches off, because $V_{GS} < V_T$
- **Therefore, the photodiode can only be reset to a voltage of ($V_{DD} - V_T$)**
  - » this limits the dynamic range of the sensor
  - » and introduces a major source of non-uniformity
  - » the trend with device scaling is shown below



- **Maybe it is time to re-assess the use of PMOS reset transistors**
  - » since device scaling reduces the impact of including the n-well

Readout

- **If we consider the readout circuit for an individual pixel**
  - » ignoring the row select transistor for the moment



- **Provided that $V_{out} > V_{bias} - V_{TL}$, L is in saturation and can be idealised by a current source, i**
  - » V_{bias} ≈1.5V, so $V_{bias} - V_{TL}$ ≈ 0.5V
  - » M is always in saturation, if $V_{diode} - V_{out} > V_{TM}$ and ignoring any body effect
- **For transistor M**

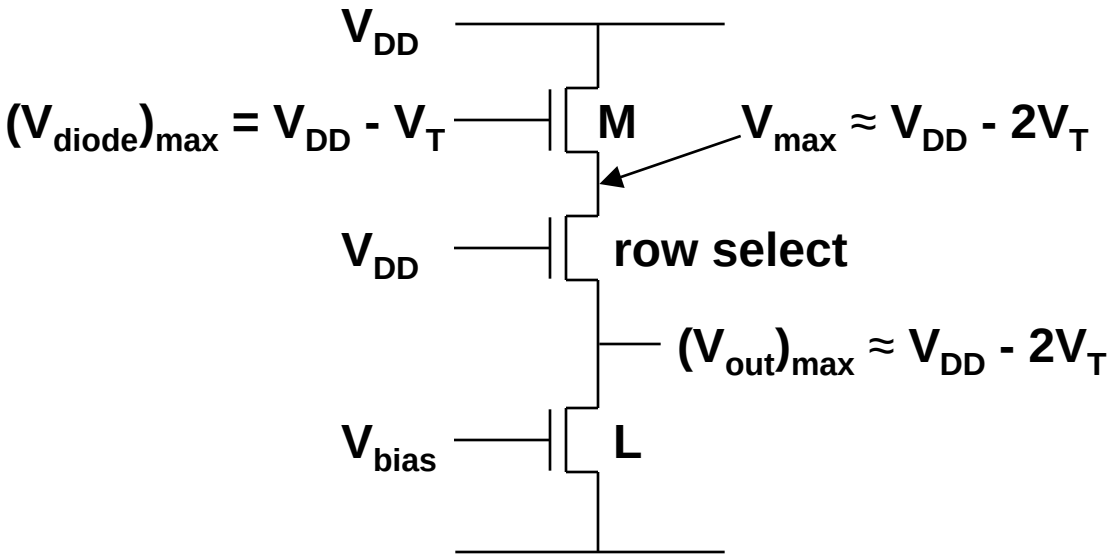
$$i = K\left[V_{GS} - V_{TM}\right]^2 = K\left[V_{diode} - V_{out} - V_{TM}\right]^2$$

$$\text{where } K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$$

- **Rearranging gives**

$$V_{out} = V_{diode} - \left(V_{TM} + \sqrt{\frac{i}{K}}\right)$$

- **The maximum possible $V_{out} = V_{diode} - V_{TM}$**
  - » or, including the reset voltage, $V_{out} < V_{DD} - (V_{TM} + V_{TR})$
  - » but this is only if i = 0
- **But otherwise, the output is linearly proportional to the diode voltage**
- **So the maximum practical output swing is**
  - » $V_{bias} - V_{TL} < V_{out} < V_{DD} - (V_{TM} + V_{TR})$
- **Hence, the bias voltage should be minimised, while still keeping the load , L, turned on**
- **From the above, we can now see that the row select transistor does not add any further voltage drop**



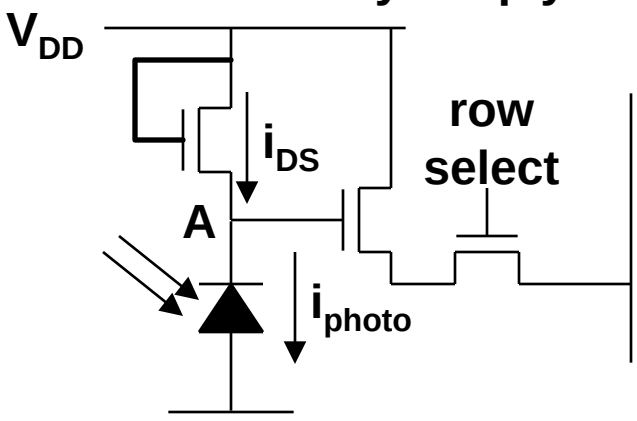
  - » even when V_{out} is at its maximum, V_{GS} for the row select is still greater than V_T so there is no further loss of signal

Typical Figures

- **For photodiode APS, the typical fill factor is about 20 – 35%**
  - » taking into account the photosensitive area as a fraction of the total pixel area
  - » pixel area = (total sensor area)/(n x m pixels)
- **The real pixel size is called the “pixel pitch”**
  - » and is the (array width) / (n columns) or (array height)/(m rows)
  - » which are not necessarily the same
- **Typically the pixel pitch ~ 15 x min. feature size**
- **The peak quantum efficiency (QE) is ~40% at green wavelengths**
- **Conversion gain ~ 3μV/e^-**
  - » which is quite low compared to CCDs and photogate
- **Saturation signal ~ 300,000 e^-**
- **Dynamic range ~ 6000:1 (75dB)**
- **The maximum commercial array size is currently about 1024 x 1024**
  - » although larger experimental devices have been reported

Log. Photodiode APS

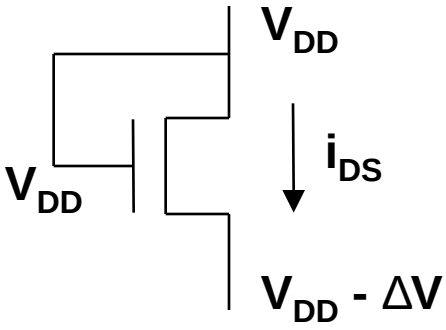
- **An interesting variant on the basic 3-transistor APS circuit allows for a logarithmic response from the sensor**
- **If the dynamic range is limited by voltage swings in the circuit, and not by the full-well of the diode**
  - » then logarithmic encoding of the photo-signal allows for a much wider dynamic range
  - » i.e. same voltage swing for a wider range of illumination
- **This can be achieved very simply**



- **Because i_{photo} is very small, the apparent resistance of the photodiode is large**
  - » and the voltage at A is only slightly lower than V_{DD}
  - » in fact, just low enough so that $i_{DS} = i_{photo}$

MOSFET in Sub-threshold

- **The bias conditions of the MOSFET are somewhat unusual**



- **Now $V_{GS} < V_T$ and the FET is officially off**
  - » except that a small “sub-threshold” current can flow
  - » the FET is in inversion, but not the strong inversion required for above threshold operation
- **In weak inversion, current flow is dominated by the diffusion of minority carriers (e^- here)**

$$i_{DS} = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L)}{L}$$

  - » where n(0) and n(L) are the electron concentrations at the source and drain, respectively, A is the area for conduction, and L is the channel length
  - » J_{drift} n, but J_{diff} dn/dy, which can be large even for low n

- **The electron concentrations are**

$$n(0) = n_{p0} \exp\left(\frac{q\psi_s}{kT}\right)$$

$$n(L) = n_{p0} \exp\left(\frac{q\psi_s - qV_{DS}}{kT}\right)$$

  - where ψ_s is the surface potential, given by $[(E_i)_{bulk} - (E_i)_{interface}]/q$

- **At the surface of the semiconductor, the electric field is**

$$E_s = -\frac{Q_{depletion}}{\varepsilon_{Si}} = \frac{qN_A W_{depl}}{\varepsilon_{Si}}$$

$$= \frac{qN_A}{\varepsilon_{Si}} \sqrt{\frac{2\varepsilon_{Si}\psi_s}{qN_A}}$$

$$= \sqrt{\frac{2qN_A\psi_s}{\varepsilon_{Si}}}$$

- **In the equation above, the area for current flow, A, equals the width of the FET x channel thickness, t_{chan}**

  - t_{chan} is defined by the point at which the electron concentration falls to 1/e of its value at the surface
  - i.e. where ψ_s is decreased by kT/q

- **This occurs at $t_{chan} = kT/qE_s$**

- **By substitution, and without doing much simplification, we get**

$$i_{DS} = D_n \left(\frac{W}{L}\right)\left(\frac{n_i^2}{N_A}\right)\frac{kT}{\sqrt{\frac{2qN_A\psi_s}{\varepsilon_{Si}}}} e^{\frac{q\psi_s}{kT}}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$

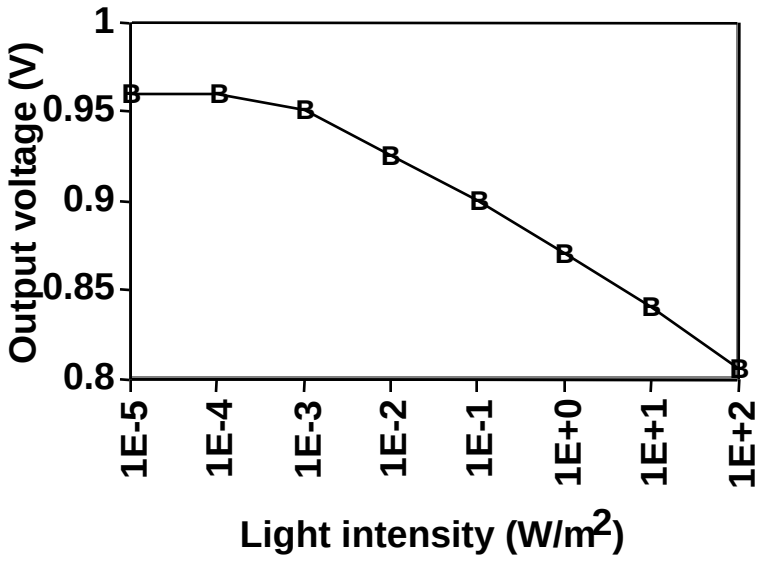
- **Now, if $V_{DS} > 3kT/q$ ($\approx 75mV$), the last term in the above equation ≈ 1**
  - » and the $\exp(\psi_s)$ term dominates, so i_{DS} = const. x $\exp(q\psi_s/kT)$
- **The surface potential, ψ_s, is given by (V_{GS} - constant terms)**
  - » and in our circuit, $V_{GS} = V_{DS}$
  - » so we find $i_{DS} = i_0 \exp(qV_{DS}/kT)$
  - » where the i_0 incorporates all the constant terms
- **Finally, by rearranging, we obtain**

$$V_S = V_{out} = V_D - \frac{kT}{q}\ln\left(\frac{i_{DS}}{i_0}\right) = V_D - \frac{kT}{q}\ln\left(\frac{i_{photo}}{i_0}\right)$$

- **So as the illumination (and hence i_{photo}) increases <u>linearly</u>**
  - » the output voltage decreases <u>logarithmically</u>

IMEC Log APS

- **Logarithmic pixels have been promoted in particular by the Inter-University Microelectronics Centre (IMEC) in Belgium**
  - » in the introduction, we saw pictures taken by an IMEC camera in space
- **IMEC is one of the leading APS laboratories and have made innovative devices such as**
  - » a “circular” foveated camera
  - » a 2048 x 2048 array
  - » a “time-to-crash” sensor
- **Below is a typical output characteristic for one of the IMEC logarithmic sensors**



Advantages of Log APS

- **The much-sought-after advantage of the log compression is that the sensor measures illumination over a range of > 5 orders of magnitude**
  - » the dynamic range is ~100,000:1 (100dB)
  - » i.e. an order of magnitude more than ordinary APS
  - » remember that an office scene may have a range of illumination of 10^6
- **In addition, the log pixels do not need a reset line**
  - » so the operation is simpler
  - » and the fill factor is higher
- **Because they use no integration time, the pixel can be read out at any time as well as in any sequence**
  - » so they are truly randomly accessible
- **So why doesn't everyone use them?**

Disadvantages of Log APS

- **While the dynamic range is large, the log pixels suffer from several serious drawbacks arising from the sub-threshold operation of the FET**
- **In the i_{DS} expression is the term in $\exp(q\psi_s/kT)$**
  - » in ψ_s are factors such as the threshold and flatband voltages, which depends on the interface conditions, and the oxide thickness, as well as the gate voltage
  - » therefore the output characteristics are sensitive to such variations at a similar level to the signal
- **The kT/q term leads to a significant temperature dependence of the output**
  - » about 8mV/°C, according to IMEC
  - » this could be a problem for large arrays where significant temperature gradients are possible
- **But the main difficulties arise because of the low swing of the output signal**
  - » only about 0.15V for 5 orders change in illumination
- **For example, FET threshold voltages can have a variation of ± 5 - 10%**
  - » i.e. about 0.1V
  - » comparable with the recorded signal levels

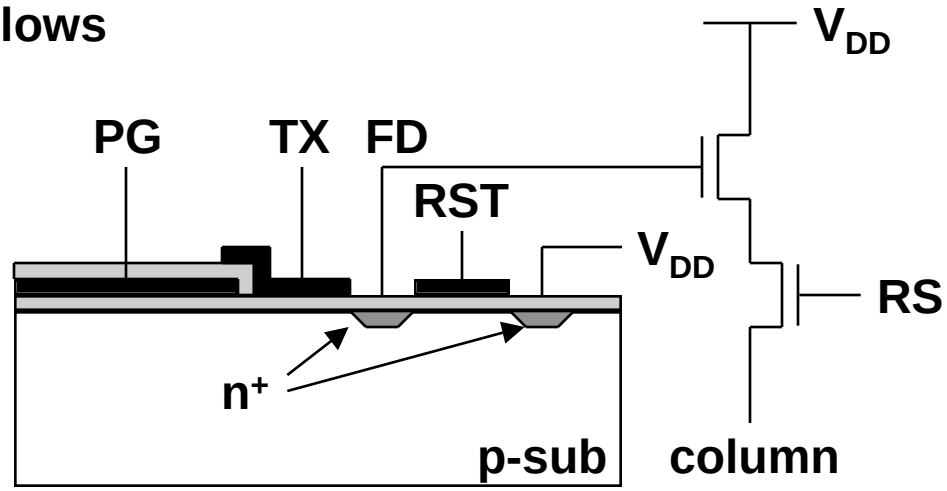
- **These variations appear as fixed pattern noise**
  - » and are so severe for log pixels that some subtraction of stored “background” signals is essential
  - » and owing to the continuous output, a correlated double sampling approach (see later) does not work and a whole array’s worth of reference values must be stored somewhere
- **Moreover, the small signals make the sensors susceptible to other noise sources**
  - » a signal-to-noise ratio of 45dB (~180:1) is typical
  - » an integrating photodiode pixel may get 55-60dB (1000:1)
- **All of this means that a fully integrated camera system using the log pixels is hard to implement**
- **The remaining issue with the logarithmic pixels is their speed at low light levels**
  - » since the only way of charging/discharging the sensing node is by means of the photocurrent
  - » which can take a long time at low i_{photo}
- **Say C_d = 2pF, i_{photo} = 10pA, and ΔV = 0.1V**
  - » so $\Delta Q = C_d \Delta V = 2.10^{-12} \times 0.1 = 10^{-13}$ C
  - » at $i_{photo} = 10^{-11}$ C/s, it takes ~10ms per pixel to remove the charge (i.e. 100 pixels/s maximum readout rate)

Photogate APS

- **Photogate Active Pixel Sensors were developed in the early 1990s by workers at the Jet Propulsion Laboratory (JPL), part of NASA**
- **The design of photogates owes a lot to CCD techniques**
  - » indeed, the photogate looks just like the final stage of a CCD register
- **The structure and operation are more complex than for the photodiodes, but they offered several advantages:**
  - » not previously patented!
  - » (now patented by Eric Fossum of JPL)
  - » allows improved noise suppression (see later)
  - » and a greater Q → V conversion efficiency, due to its separate output node
- **The main disadvantage is that their quantum efficiency is reduced by the use of an overlying poly-Si gate**
  - » the advantage of conversion efficiency is almost exactly offset by the reduced QE

Operation of Photogate

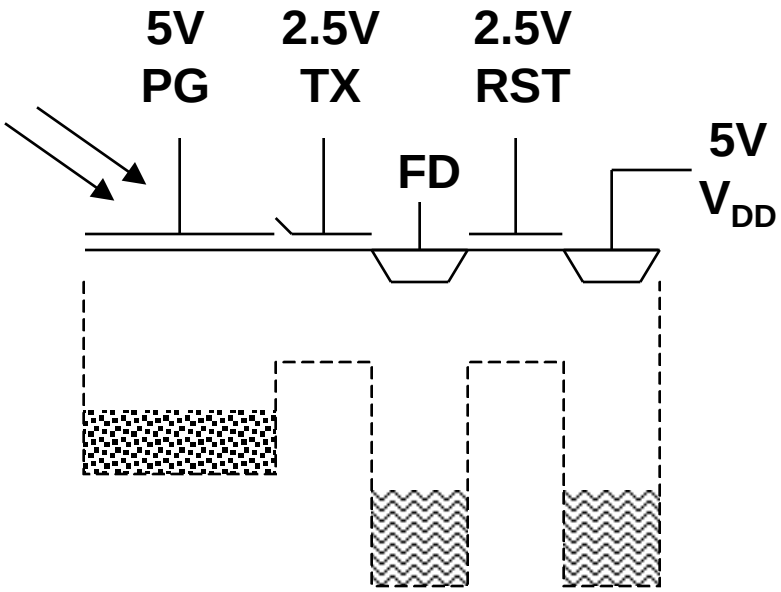
- **The schematic of the photogate pixel is as follows**



- **The photogate (PG) is biased positively, thereby creating a potential well in the deep-depleted substrate**
  - » thereby providing storage for the photo-generated charge
- **A transmission gate (TX) is dc biased during integration and acts like a surface-channel CCD**
  - » when the PG is pulsed to 0V, charge is transferred under the TX gate to the floating diffusion output node
  - » ideally, the TX gate should overlap the PG to ensure effective charge transfer (i.e. a double-poly process)

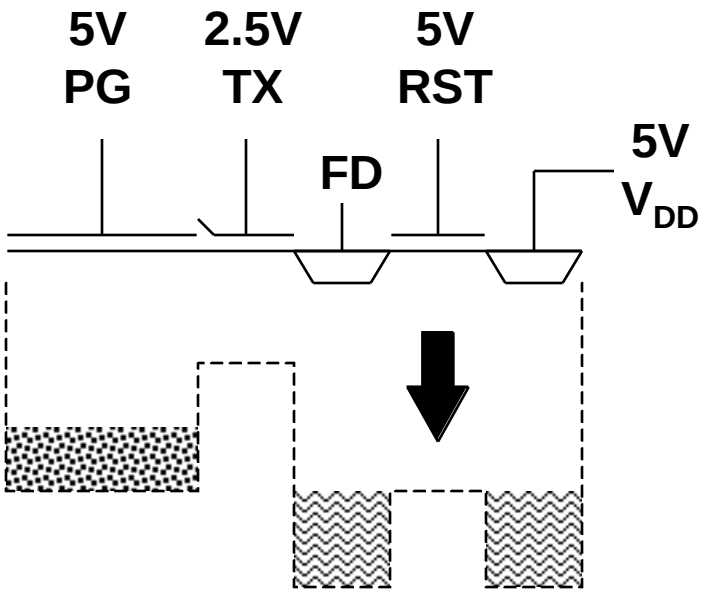
- **The floating diffusion (FD) acts as the charge-voltage conversion node**
  - » and the signal is read out using the conventional source-follower circuit
  - » a typical capacitance is 10fF, giving a conversion efficiency of 10–20 μV/e^-
- **This floating diffusion is reset (RST) by the neighbouring reset FET**
- **The added complexity of the pixel reduces the minimum dimensions to ~20 times the process feature size**
  - » so 10μm for a 0.5μm process
  - » with a fill factor that is somewhat lower than that for a photodiode
- **Because of the overlying poly-Si gate, the quantum efficiency is lower than a photodiode, especially at the blue end of the spectrum**
  - » typically the peak value ~20%
  - » compared with 35-40% for photodiode
- **A typical operating sequence for the photogate pixel is described below**

1. Signal Integration



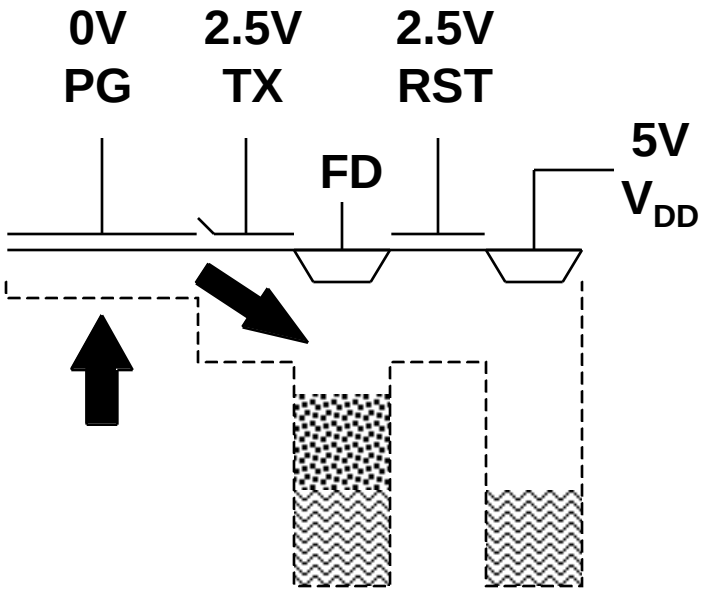
- **TX and RST are biased lower than PG to provide for some lateral antiblooming control**
  - » both from PG to FD
  - » and from FD to V_{DD}
- **This ensures that any charge spilling over from a full well is not allowed to flow into adjacent pixels**

2. Reset



- RST is pulsed to 5V, in order to reset the FD to ~3.5V
- The final reset voltage is V_T lower than V_{DD}
- FD is reset immediately before the signal readout because this allows improved noise reduction

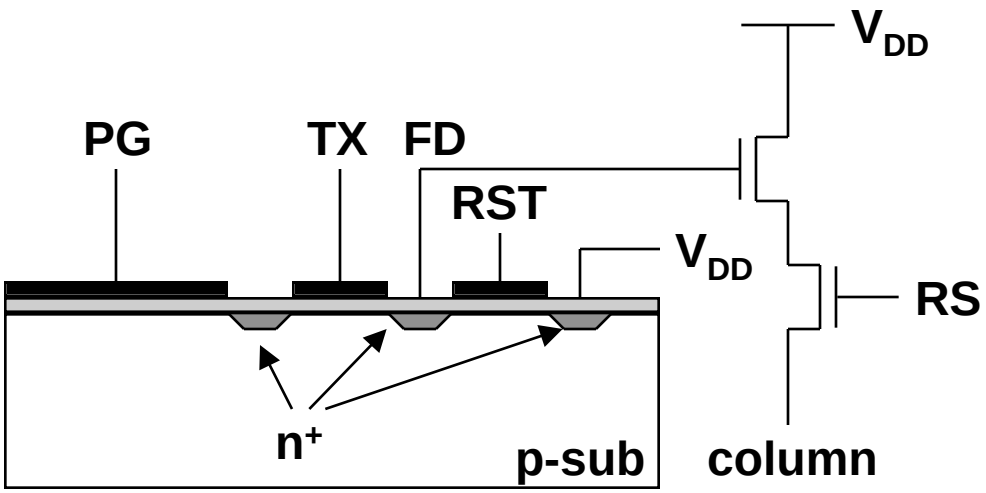
3. Charge Transfer



- **Now, PG is pulsed to 0V to transfer the charge via TX onto the FD**
- **Calculated full well capacities are on the order of 10^6 e^-**
  - » although this, of course, depends on the gate area
  - » but the realisable value depends on the output circuitry, such as the transistor biasing
- **The signal charge is <u>added</u> to any charge remaining after the reset operation**

Single-poly Photogate

- While double-poly is a feature of many analog CMOS technologies, its use does restrict the generality of the design
- However, the need for overlapping gates can be removed by adding an intermediate “bridging” diffusion



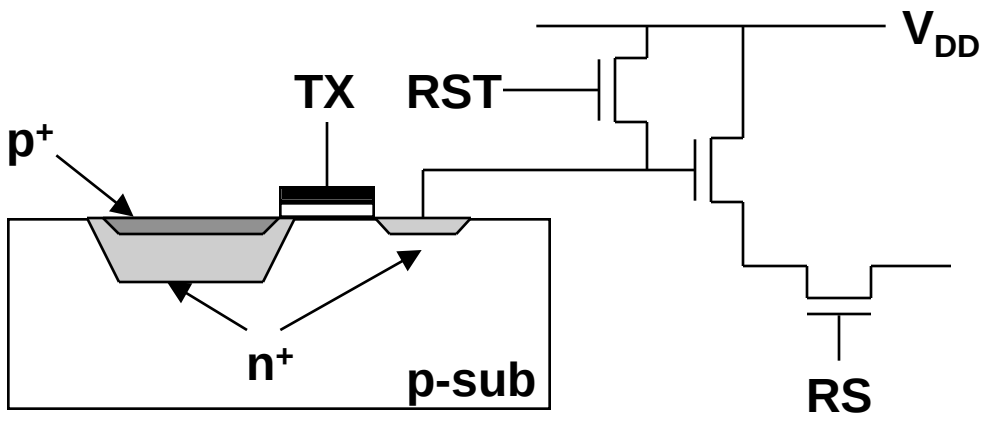
- Save for the possible introduction of some image lag, the use of this extra diffusion has little affect on the performance of the pixel

Pinned Photodiode

- **While the pinned photodiode is not strictly related to the photogate, it bears some similarity in operating principle**
  - » and was originally developed with CCDs in mind
- **This structure is intended to give an improved quantum efficiency in the blue region of the spectrum**
  - » and a lower dark current
- **The device uses additional implantation steps to the standard CMOS process to optimise the performance of the photodetector**
  - » and has been commercialised by Eastman-Kodak and Motorola under the name of ImageMOS™
  - » and patented
  - » it is this kind of “tweaking” of the standard CMOS process that Wong believes will become the norm for integrated image sensors
- **Pinned photodiodes were first proposed for CCD sensors in the early 1980s and applied to a combined CMOS/CCD structure in 1995 in a JPL/Kodak collaboration**

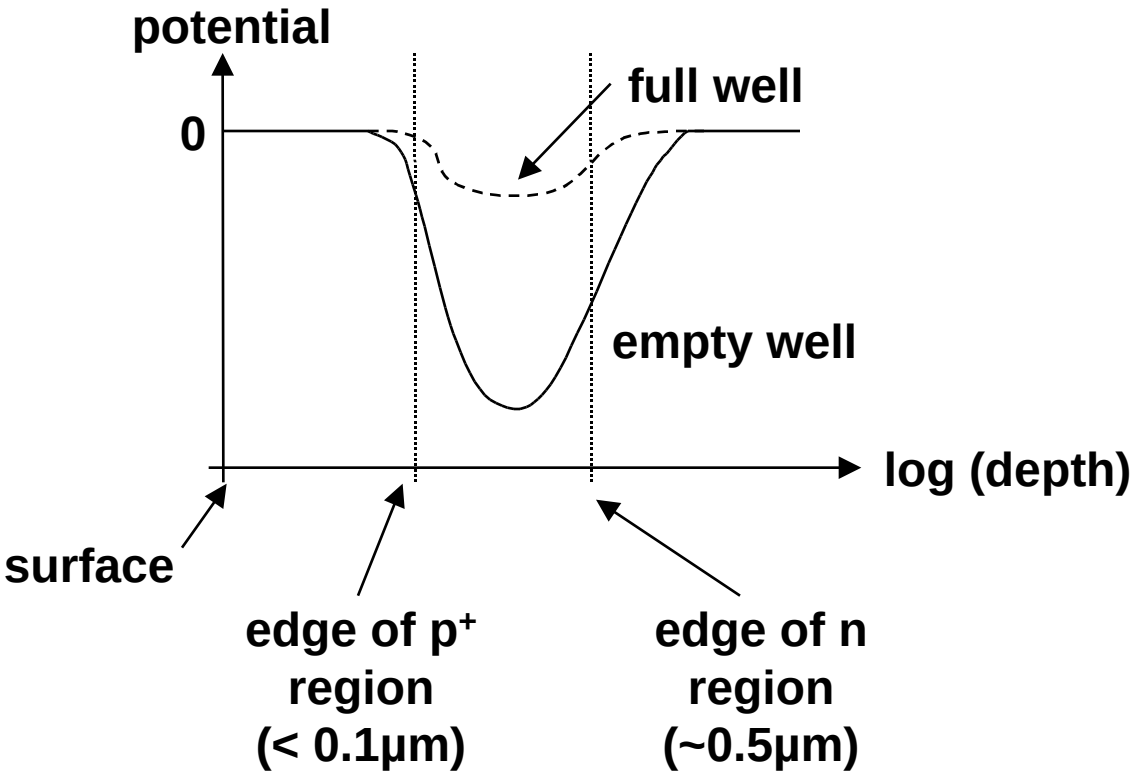
Structure of Pinned PD

- **The pinned photodiode is just like a regular photodiode**
  - » except for an additional p^+ surface implant



- **The p^+ implant acts rather like a self-biased, internal photogate**
- **Doping levels and implant depths must be carefully controlled**
  - » to deplete the n-region fully
  - » to ensure effective charge transfer from the diode to the floating diffusion
- **The name "pinned diode" arises because the p^+ implant pins the potential at the surface to that of the substrate**

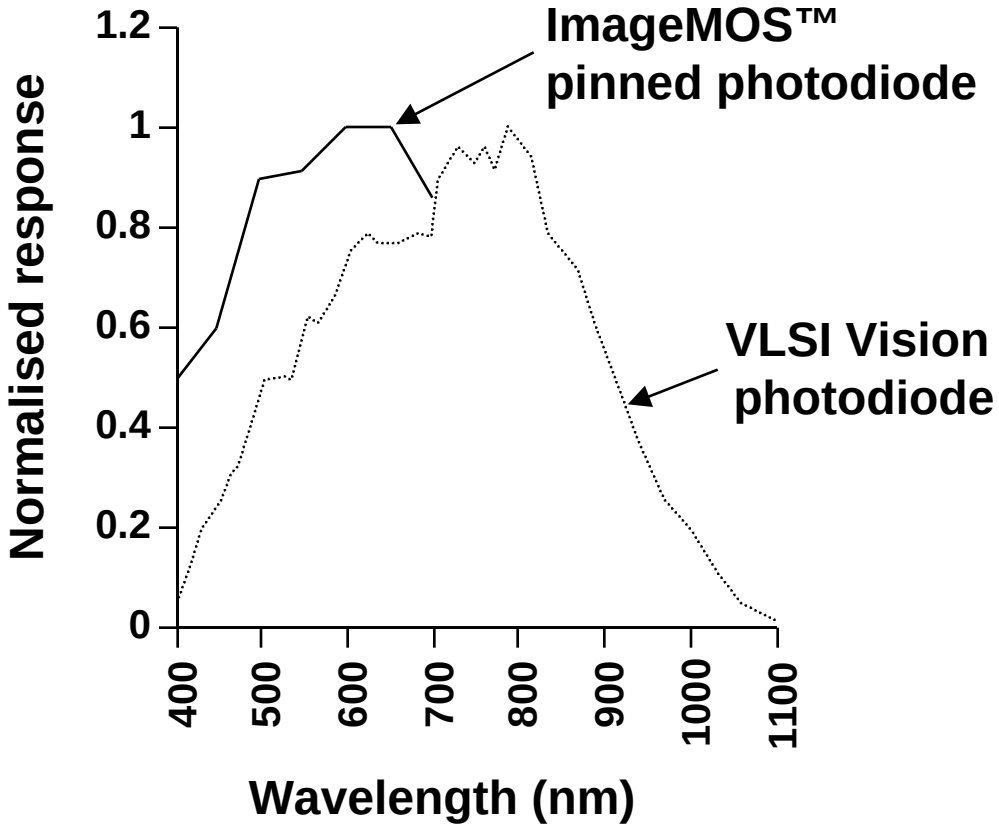
- **So the potential, as a function of depth, looks like**



- **The operation of the pixel is similar to that of the photogate**
  - » the FD is reset
  - » TX is used to transfer the signal charge onto the FD
  - » the diode itself is reset through RST and TX
- **The ImageMOS™ process is based on a 3.3V 0.6µm CMOS technology**
  - » the output voltage swing at the output is ~650mV, and is the limiting factor on the dynamic range

Spectral Response

- **Part of the purpose for using pinned diodes is to increase the pixel responsivity at short wavelengths**
- **This is mainly as a result of a reduced surface recombination of photo-generated e-h pairs**
  - » arising from the doping profile a short distance beneath the surface
  - » which creates a field favourable for e-h pair separation



Dark Current

- **Dark current in the depletion region of a conventional p-n junction is dependent on the volume of material in which thermally generated e-h pairs can be collected**

$$J_{dark} = \frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}$$

- **So the width of the depletion region is important**
  - » as determined by n_{p0} and p_{n0}, the minority carrier concentrations
  - » which are in turn affected by the doping concentrations
  - » so the depletion region is smaller for higher doping
- **And the rate and distance of the diffusion of minority carriers**
  - » which also decrease for higher doping
- **In general, however, the same volume must also be maximised to achieve the efficient collection of photo-generated charge**
- **Although geometrical effects, perimeters etc. also influence J_{dark}**

- **But if we can tailor the sensor such that the depletion region is at the correct depth for efficient optical absorption**
  - » the depletion region does not have to be so large
  - » and the dark current can be reduced
- **For the ImageMOS™, the dark current is better than for a regular photodiode**
  - » by a factor of ≥ 2
- **The profile of the p^+ implant right at the surface also reduces the collection of dark current generated at the surface states at the Si-SiO_2 interface**
- **Fill factor is reduced by the transmission gate, but this also provides some anti-blooming function**
- **It is not yet clear how "revolutionary" the use of pinned diodes will be for CMOS image sensors**
  - » technology is less widespread
  - » more complex pixels

Summary

- **This has covered all of the common CMOS compatible photosensors**
- **In the search for the perfect performance, other sensors have been proposed**
  - » such as lateral BJTs, fabricated using CMOS technology
  - » charge injection devices (CID)
  - » charge modulation device (CMD) which have achieved success for HDTV cameras
- **But the photodiode and charge-transfer based pixels are by far the most widespread**
  - » the “specialised” designs are frequently promoted by single companies
  - » either for proprietary reasons or for specialised applications
- **It is likely that new designs will proliferate as the rigid link to standard CMOS is severed**
  - » either by choice for performance enhancements
  - » or forced by the continued scaling of the CMOS process

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