A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13µm Technology for RF SoC Applications

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***Abstract*—An integrated low-noise, high power supply rejection ratio (PSRR), low-dropout (LDO) linear regulator has been developed in Texas Instruments' (TI) 130nm CMOS technology. The LDO regulator is capable of producing a regulated output voltage of 2.8 V from a Li-Ion battery supply, with a dropout voltage of 200 mV while supplying a load current of 150 mA. The LDO regulator features > 65 dB PSRR at 20 kHz, and > 40 dB up to 1 MHz. The LDO regulator also features output noise performance of < 350 $nV_{rms}/\sqrt{Hz}$ at 100Hz. The LDO die area is 0.166 mm^2 and the maximum no-load power consumption is 450 µW.**

I. INTRODUCTION

SoC architectures, which now often feature power management functionality integrated with the DBB, ABB, and sometimes RF, present the circuit designer with new challenges, even for very well known circuit architectures. As high-voltage, analog friendly process technologies are replaced with digitally dense, deep-submicron technologies, the power management designer must adapt circuit techniques without sacrificing the integrity of the design. To complicate matters more, customers are unwilling to relax specified tolerances due to limitations of the deep-submicron processes.

Presented is an integrated low-noise, high-PSRR LDO in deep- submicron. The LDO is capable of driving both on- or off-chip RF loads. The motivation of this paper is several-fold: To provide the audience an overview of the capabilities and limitations of 130nm CMOS technology in relation to direct-battery connect power management circuit design, to discuss and analyze techniques and methods of low-noise, high-PSRR LDO design, and to present silicon data from a leading-edge SoC RF LDO application.

II. PROCESS OVERVIEW

The technology used, TI's 130nm process, is a process tailored for very high digital density mixed-signal integration applications. It is a single poly, 3 metal process, capable of producing excellent digital gate density for digital applications. For analog applications, especially power management, this technology also introduces more design challenges due to the limitations of the deep-submicron devices. The key limitations are low device operating voltage rating and high device leakage. The primary devices employed in this particular design are the 1.5V core devices and the 5V drain-extended devices (DEMOS). Both devices have a 32Å gate and the gate-to-source voltage is 1.5V rated. DEMOSs have a 5V drain-to-source rating. The capacitor types used in this design include 1.5V and 3.3V depleted MOSFET capacitors.

III. DESIGN CONSIDERATIONS AND ARCHITECTURE

The LDO regulator presented is designed for noise and power supply rejection (PSR) performance. The following section will discuss the architecture for this LDO regulator design in more detail.

A. Power FET Design

The power FET structure used in this design is illustrated in Fig. 1. The power FET is constructed by cascoding a DEPMOS with a core device, where the DEPMOS is biased by Pbias. The cascoded structure protects the core device from voltage stress. The core device at the top can operate in or close to the saturation region during most of the input voltage conditions. As a result, the output impedance of the power FET is higher; therefore, better power supply rejection is achieved. This structure also brings in another benefit of cascoded device, which is reducing the parasitic that needs to be driven by the gate driver. Smaller parasitics help simplify the regulator compensation.

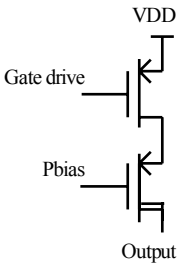

Fig. 1. Power device structure.

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B. LDO Regulator Architecture Overview

This regulator is a four stage single ended amplifier as depicted in Fig. 2. It is an internally single Miller Capacitor (SMC) compensated high gain system. Similar SMC compensation techniques for multi-stage amplifier have been discussed in [1] and [2]. The Miller compensation provides a better control of the stability over a large output capacitor variation (refer to TABLE I.). At the same time, it also produces a better load transient response since the Miller capacitor is a high frequency negative feedback that directly couples to the output. The high gain configuration enables this LDO regulator to have superior DC line and Load regulation. However, the test result for this design is showing more than 10mV load regulation. Since a dedicated output sensing pin is not available, the achievable DC load regulation performance is limited by the parasitic of the bond wire and the package substrate. The DC IR voltage drop across the package parasitics will directly degrade the DC load regulation performance.

Referring to Fig. 2, the basic structure of this LDO regulator consists of four gain stages. The first stage serves as a differential to single ended gain stage, while the second, third, and fourth gain stages are all single ended. There is a Miller capacitor, C1, connected across the last three stages to serves as the primary compensation. By design, the top plate of C1 is connected to a node that is ground reference. This configuration will isolate supply noise from coupling into the critical nodes via the Miller capacitor. The second and third stages are wideband stages. The wideband characteristics are required to ensure that the LDO regulator remains in the stable condition. At the same time, the wideband characteristics of the second and the third stage amplifier are also needed to sustain the output impedance of the power device over a wide range of frequency to achieve good power supply rejection performance.

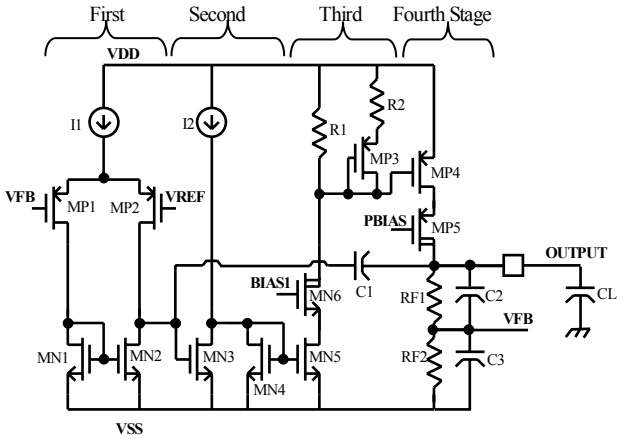

Fig. 2. Simplified architecture of the LDO.

C. LDO Regulator AC compensation

Structure wise, the second, the third, and the fourth stage can be considered as one single composite amplifier. Base on this idea, Fig. 2 can be redrawn as a functional diagram shown in Fig. 3. A1 is the first stage of the LDO regulator, while the second, third, and the fourth stages are labeled as A2, A3, and A4 respectively. The composite amplifier, which is formed by A2, A3, and A4, is depicted as A2". Compare to a two stage Miller compensated amplifier, the gain bandwidth (GBW) of the LDO regulator can be written as:

$$GBW = \frac{gm_1}{C_1} \qquad (1)$$

where gm_1 is the transconductance of the first stage, A1. As indicated, GBW is not dependant upon the output capacitor (CL). The dominant pole of the system, P_1, can be written as:

$$P_1 \approx \frac{1}{R_{o1} \cdot A2'' \cdot CL} \approx \frac{1}{R_{o1} \cdot A2 \cdot A3 \cdot A4 \cdot CL} \qquad (2)$$

where R_{o1} is the output impedance of A1. Similar to two-stage Miller capacitor compensated amplifier, the second composite amplifier A2" is expected to have an AC response that is close to a single pole system. After the pole splitting introduced by the Miller compensation, if the dominant pole for A2"is located at its output, the second pole, P_2, can be approximated as:

$$P_2 \approx \frac{gm_2''}{CL} \approx \frac{A2 \cdot A3 \cdot gm_4}{CL} \qquad (3)$$

Where gm_2" is the transconductance of A2" and gm_4 is the transconductance of A4. To make the dominant pole for A2" always at its output, the output poles of the second and the third stage amplifiers have to be moved to a significantly higher frequency range than where P_2 is located. To ensure stability, the dominant pole of A2" is required to remain at the output.

Since this system is used as a LDO regulator, the output current is expected to change between zero and full load; therefore, gm_4 is expected to change accordingly. As a result, P_2 will move based upon the value of the output load current. To compensate for this scenario, A3 is dynamically biased according to the load current condition. At heavy loading conditions, A3 is biased more heavily to widen its bandwidth and to reduce its output impedance to adapt to P_2 moving to higher frequency. At light loading conditions where P_2 is at lower frequency, a narrower A3 bandwidth and higher A3 output impedance can be tolerated for stability. Lighter bias is used to keep the power consumption low. Similar dynamic biasing compensation techniques have been presented in [3] and [4].

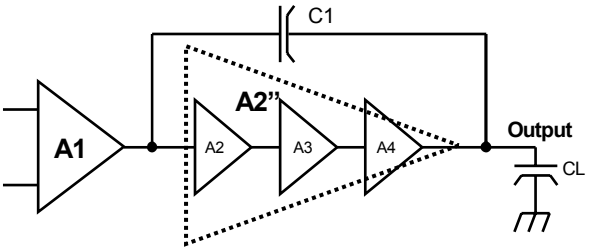

Fig. 3. AC Compensation functional diagram.

D. LDO Regulator Architecture Detail

The first stage of the LDO regulator is a differential input gain stage constructed by MP1, MP2, MN1, MN2, and I1. For the noise performance of a LDO regulator, the first stage is

always the most critical stage. The noise contributed by the next three stages will be attenuated by the first gain stage; therefore, their noise performance is secondary in consideration. For low noise, the physical sizes of these four transistors, especially the differential pair (MP1 and MP2), in the first stage is designed to be large enough to keep the flicker noise low. For the thermal noise, the transconductance (g_m) of the transistors needs to be kept high since the g_m of a transistor is inversely proportional to its generated thermal noise. In this case, the g_m of the differential pair is the key for noise reduction since the noise will not be attenuated. Therefore, the bias current I1 is set so that the input transistors, MP1 and MP2, can produce sufficient g_m to keep the noise low. The W/L of MP1 and MP2 are biased to the sub-threshold region so that maximum g_m can be generated for the given I1.

The second stage is a wideband common source amplifier formed by MN3, MN4, and I2. The diode connected MN4 at the output provides a low impedance path to ground. As a result, the gain stage manages to push the output parasitic pole to a high enough frequency to keep it from interfering with the Miller compensation. This stage is intentionally made to be a gain stage with ground reference input, so that the top plate of the Miller capacitor C1 can be connected to a ground reference node to avoid any significant coupling from the power supply degrading the PSR performance.

The third gain stage is also a common source amplifier. The g_m of this stage is generated by MN5 with MN6 cascoded on top. MN6 not only serves as a voltage stress protection device, it also increases the impedance to ground at the output node significantly. Since the output of this stage is connected to the gate of the power PMOS MP4, this node is designed so that the impedance to ground is significantly larger than the impedance to VDD. It allows the gate of MP4 to track VDD fluctuation better so that good PSR performance can be achieved. To produce a low impedance path to VDD, the load of this stage is constructed by a resistor R1 and PMOS MP3 in series with a resistor R2. When the LDO regulator output current is very low, the power device MP4 will be operating in the sub-threshold region. As a result, the V_{GS} of MP4 will be lower than a V_t. Since this V_{GS} is the same as the V_{GS} of MP3, MP3 is virtually turned off. Under this condition, R1 is the only biasing source for MN5. When the LDO regulator is heavily loaded, the V_{GS} of MP4 increases, MP3 is turned on and switches in a very low impedance path, implemented with resistor R2. Essentially, MP3 is acting as a switch. During this condition, the impedance to VDD is greatly reduced. At the same time, the bias current for MN5 increases, the bandwidth of this stage increases. In terms of loop stability, this configuration allows the LDO regulator to adapt to the load changes by dynamically changing the bandwidth and impedance at the gate; therefore, the parasitic pole present at this node can be shifted to higher or lower frequency accordingly.

The last stage of the LDO regulator is the output stage of the regulator. The power device is realized as a combination of the core device MP4 and the DEMOS device MP5 as discussed before. The power device is driving an external filter capacitor CL and the feedback network. The feedback network consists of a voltage divider formed by RF1 and RF2, plus a capacitor divider formed by C2 and C3. The resistive voltage divider at the output of the LDO regulator acts as a noise source; the poly resistors, RF1 and RF2, contribute significant amount of flicker noise and thermal noise directly to the output. The flicker noise can only be reduced by increasing the physical dimension of the resistors, and the low frequency thermal noise produced is suppressed by keeping the resistor values small. In addition, the capacitor C2 and C3 are placed in parallel with the resistor network to filter the high frequency noise above 300KHz. AC wise, the capacitor divider also improves the high frequency response of the feedback network.

IV. MEASURED DATA

The LDO regulator was realized in silicon on a test chip. A die photomicrograph of the test chip is shown in Fig. 4, and the presented LDO regulator is highlighted. There are two bondwires per power terminal. A summary of the LDO regulator design parameters is given in Table 1. The input voltage range is from 3.0V to 4.5V. The load capacitance range is from 0.3µF to 2.7µF, with an equivalent series resistance (esr) of as little as 0 ohms.

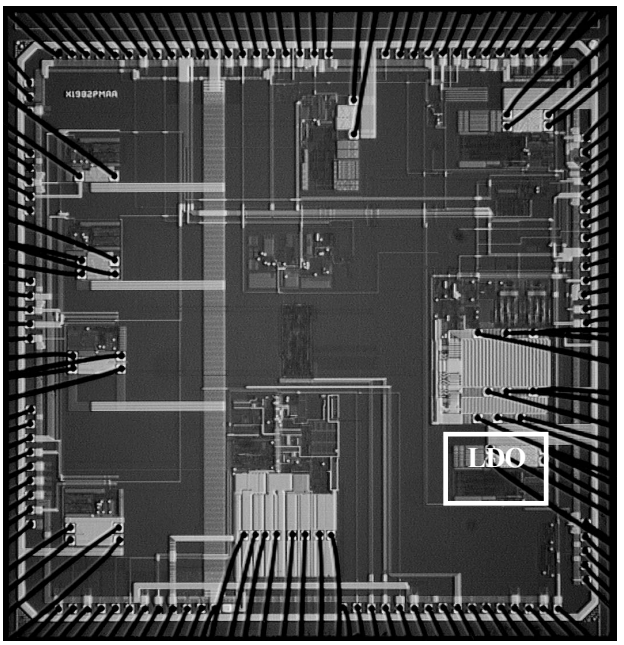

Fig. 4. Die photomicrograph of the LDO testchip.

TABLE I. SUMMARY OF THE LDO DESIGN PARAMETERS.

Parameter	**Min.**	**Typ**	**Max**	*Units*
Input Voltage	3.0	3.6	4.5	*V*
Load Current			150	*mA*
Output Capacitance	0.3	1	2.7	*µF*
Output Capacitance esr	0	10		*mΩ*

A summary of the LDO performance over temperature (-30 ºC to +85 ºC) is shown in Table 2. The DC output voltage accuracy was measured at +/-1.3%, with the majority of the error coming from the internal bandgap reference. The PSRR frequencies of interest are at 20 kHz for audio integrity of

the loads, and at 1MHz, to insure the capable rejection of on-board or pre-regulating Buck DC/DC converters. A representative plot of the LDO regulator PSRR over temperature is shown in Fig. 5. The output noise voltage of the LDO regulator is specified over three frequency ranges from 100Hz to 10MHz. A graph of the measured output noise at room temperature is shown in Fig. 6. The noise floor of the measurement, along with the noise floor of the device with the regulator off is also shown for comparison. The DC load regulation of the LDO regulator is 17.4 mV, worst case. Due to the high-gain architecture of the regulator, the majority of the load regulation error is due to the internal IR voltage drop across the bondwire and BGA substrate routes. The transient load regulation performance, which is specified at a load slew of 60mA/µs from zero to full load is -15.8 mV. The output capacitor used for this measurement was approximately 1µF. The DC line regulation was measured to be 1.5 mV. The worst-case measured dropout voltage is 199mV. The ability to integrate and optimize the bondpads within the cell was a must-have in order to reduce the parasitic layout resistance and keep the power FET area reasonable. The no-load power is measured at 441 mW at maximum input voltage of 4.5V.

TABLE II. SUMMARY OF MEASURED LDO PERFORMANCE

Parameter	**Spec**	**Measured**	*Units*
Output Voltage Accuracy	+/- 2	+/-1.3	*%*
PSRR *f* = 20kHz *f* = 1MHz	65 40	67 40	*dB*
Output Noise Voltage 100Hz – 5kHz 5kHz – 400kHz 400KHz-10MHz	350 125 20	338 100 25	*nV/√Hz*
Load Regulation	20	17.4	*mV*
Transient Load Regulation	+/- 40	+3.5, -15.8	*mV*
Line Regulation	3	1.5	*mV*
Dropout Voltage	200	199	*mV*
Power (no load)	450	441	*µW*

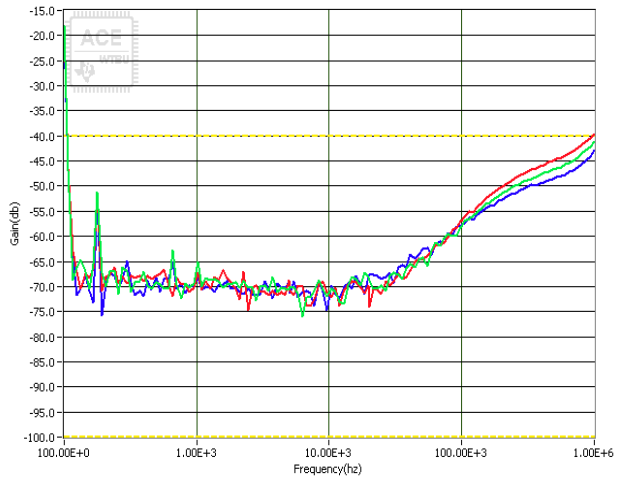

Fig. 5. Measured PSRR of the LDO over temperature.

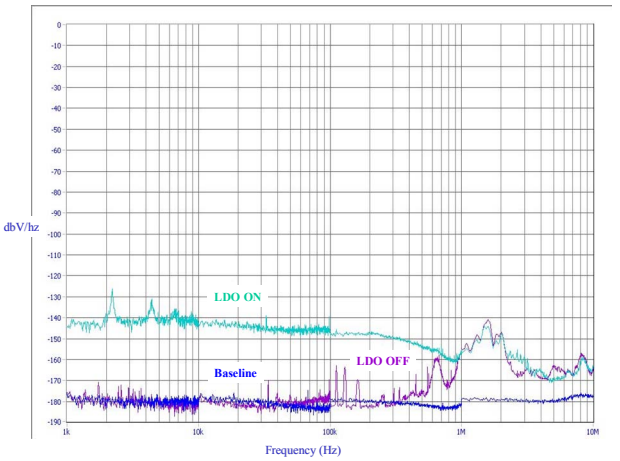

Fig. 6. Measured Output Noise of the LDO.

V. Conclusions

Presented was a low-noise, high-PSRR LDO linear regulator. The regulator was fabricated in TI's 130nm process. A brief overview of the process was given, and process-driven challenges and concerns to the analog power management designer highlighted. Techniques used to design low-noise LDOs, with an emphasis on deep submicron design, were discussed. Silicon measured results of the LDO regulator were also presented, showing proof of concept.

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REFERENCES

[1] M. Loikkanen, J. Kostamovaara, "High current CMOS operational amplifier," in *IEEE International Symposium on. Circuits and Systems*, Vol. 1, pp. 216-219, 2005.

[2] X. Fan, C. Mishra, abd E. Sanchez-Sinencio, "Single Miller capacitor compensated multistage amplifiers for large capacitive load applications," *IEEE International Symposium on Circuits and Systems*, pp. 493-496, 2004.

[3] X. Xi, "Ultra-low quiescent current low dropout (LDO) voltage regulator with dynamic bias and bandwidth," US Patent, US 6,806,690 B2, Oct.19, 2004.

[4] G. A. Rincón-Mora, P. E. Allen, "A Low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36-44, Jan 1998.