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Analog CMOS peak detect and hold circuits. Part 1. Analysis of the classical configuration[☆]

Gianluigi De Geronimo*, Paul O'Connor, Anand Kandasamy

Brookhaven National Laboratory, Instrumentation Division, Bldg 535B, Upton, NY 11973, USA

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Abstract

Peak detectors (peak-detect-and-hold circuits, PDHs) are a key element in nuclear electronics signal processing and have been incorporated as a fully integrated block in several front-end readout chips. In CMOS designs, the PDH uses an MOS current source as the rectifying element inside the feedback loop of a high-gain amplifier. However, the non-idealities in the amplifier and feedback elements significantly limit its accuracy and stability.

This paper reports on the limits of the classical CMOS PDH. Static errors due to offset, finite gain, and common-mode rejection, dynamic errors due to parasitic capacitive coupling and slew rate, and loop stability are analyzed. Expressions for each error source and consequent design tradeoffs between accuracy, speed, and dynamic range, and driving capability are derived. In a related article (Part 2), a two-phase PDH configuration, which overcomes the major limits of the classical approach is presented. © 2002 Elsevier Science B.V. All rights reserved.

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1. Introduction

Analog peak detectors (peak detect and hold (PDH), also known as peak stretchers) are important in pulse-processing circuits, where it is impractical to digitize the entire waveform. Peak detection is also used in automatic gain-control loops in communication circuits. Fast and accurate peak detectors have been developed using

discrete components, and monolithic designs have also been reported [1–8]. However, the imperfections of monolithic technology (particularly CMOS) compromise the performance. Amplifier offset, finite gain, poor common-mode rejection, low slew rate, and parasitic capacitance all affect the accuracy of the peak-height measurement.

In this paper, we analyze the classical CMOS PDH (and its variations) based on a MOSFET current source as the rectifying element in the feedback loop of a high-gain amplifier. The error sources are grouped into two classes, static and dynamic. Along with accuracy, we consider the impact of each error source on speed, stability, dynamic range, and driving capability. In Section

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*Corresponding author. Tel.: +1-516-344-5336; fax: +1-516-344-5773.

E-mail address: degeronimo@bnl.gov (G. De Geronimo).

2.1, we discuss the basic schematic and operation of the CMOS PDH. In Section 2.2, we analyze the static and dynamic sources of inaccuracy stemming from imperfections of the rectifying current source and high-gain amplifier. Section 2.3 discusses the feedback loop stability and compensation schemes. In Section 2.4, the output-driving capability of the PDH is examined, and in Section 2.5, we comment on the current state-of-the-art.

In a related article [9], we present a two-phase configuration, which overcomes the major limits of the classical PDH.

2. Analysis of the classical CMOS PDH

2.1. PDH operation

A simplified schematic of the classical CMOS PDH circuit for positive voltage pulses is shown in Fig. 1. The analysis, which follows concerns PDH for positive voltage pulses, but it can be easily extended to the case of negative voltage pulses.

The p-MOSFET M_1 acts both as a charging and as a switching element. When a pulse $V_i(t)$ arrives and is higher than the hold voltage V_h , the error signal $V_e(t) = V_h(t) - V_i(t)$ at the input of amplifier A, generates a sharp negative transition of the gate voltage V_g that switches M_1 on. A current $I_d(t)$ then charges the hold capacitor C_h until $V_e(t)$ approaches zero. The gate voltage $V_g(t)$ is then continuously adjusted by the loop to give $I_d(t) = C V_i'(t)$, where $V_i'(t)$ is the slope of $V_i(t)$. The

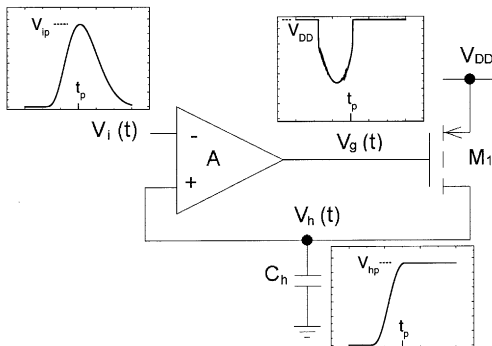


Fig. 1. Simplified schematic of the classical CMOS PDH circuit for positive voltage pulses.

tracking condition $V_h(t) = V_i(t)$ persists until $V_i(t)$ approaches its peak value $V_i(t_p) = V_{ip}$, when $V_i'(t)$ goes to zero. Then, the error signal $V_e(t)$ changes sign and generates a sharp positive transition of V_g that switches M_1 off. Since there is no discharge path available for C_h , $V_h(t)$ retains the peak value of $V_i(t)$. The hold condition with $V_h(t > t_{pk}) = V_{hp} = V_{ip}$ is thus achieved. Examples of the signals $V_i(t)$, $V_g(t)$ and $V_h(t)$ are shown as insets in Fig. 1.

2.2. Error analysis

The accuracy of the classical CMOS PDH can be affected by the non-ideality of M_1 and A, which contribute in several ways to the total error $V_{ep} = V_{hp} - V_{ip}$. The individual error mechanisms will be discussed in Sections 2.2.1 and 2.2.2.

2.2.1. Errors due to M_1

The MOSFET M_1 introduces errors through the gate-to-drain capacitive coupling C_{gd} , the part of the channel charge Q_{ch} injected into the drain node (hold node), and the dependence of the drain capacitance C_d on the drain voltage V_h and drain current I_d (see Fig. 2).

In order to evaluate these errors, M_1 must be suitably sized, which requires that the maximum drain current $I_{d,max}$ of M_1 must charge C_h (assumed to be $\gg C_d$ and C_{gd}) with a slew rate equal to the maximum expected slope $V_i'_{max}$ of the input pulse $V_i(t)$:

$$C_h V_i'_{max} = I_{d,max} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{DD} - V_g - V_T)^2 \tag{1}$$

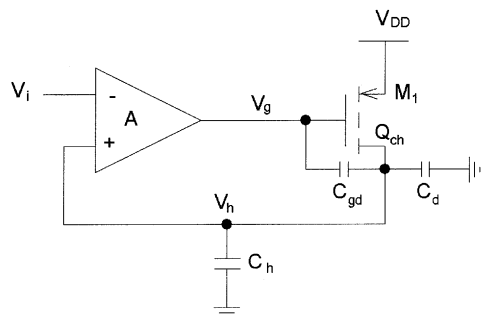


Fig. 2. Schematic of the PDH showing sources of error from M_1 .

where W and L are the channel width and length of M_1 , respectively, V_T is its threshold voltage (absolute value), μ_p is the hole mobility, and C_{ox} is the gate oxide capacitance density. From Eq. (1) and imposing $V_{g,\min} = 0$ (the limiting case), it follows that

$$\frac{C_{ox}WL}{C_h} \approx \frac{2V'_{i,\max}L^2}{\mu_p(V_{DD} - V_T)^2}. \quad (2)$$

The sharp positive transition δV_g , which occurs at the gate M_1 in proximity of the peak is coupled to the hold node through C_{gd} and it contributes an error:

$$V_{e,C_{gd}} = \delta V_g \frac{C_{gd}}{C_h + C_{gd}} \approx \delta V_g \frac{C_{ox}WL}{C_h} \left(\frac{1}{3} + \eta \right) \quad (3)$$

where we assumed $C_h \gg C_{gd} \approx C_{ox}WL/3 + C_{ov}W \approx C_{ox}WL(1/3 + \eta)$ and η is a coefficient related to the drain-overlap capacitance typically not higher than 1/5 for sub- μm CMOS technologies. The worst case occurs when the input pulse has the maximum slope ($V'_{i,\max}$) and a triangular peak shape. Assuming this worst case input pulse, $\delta V_g = V_{DD}$ and it follows from Eq. (2) that

$$V_{e,C_{gd}} \approx V_{DD} \frac{2V'_{i,\max}L^2}{\mu_p(V_{DD} - V_T)^2} \left(\frac{1}{3} + \frac{1}{5} \right). \quad (4)$$

The part of the channel charge Q_{ch} injected into the hold node contributes an error, which can be evaluated from $Q_{ch} \approx C_{ox}(V_{DD} - V_g - V_T)$ and by assuming that about 1/3 of this amount affects the hold node. It follows from Eq. (2) that

$$\begin{aligned} V_{e,Q_{ch}} &= \frac{Q_{ch}}{C_h} \frac{1}{3} \approx (V_{DD} - V_T) \frac{C_{ox}WL}{C_h} \frac{1}{3} \\ &= \frac{2V'_{i,\max}L^2}{\mu_p(V_{DD} - V_T)^2} \frac{1}{3} \end{aligned} \quad (5)$$

where we assumed again the worst case of a triangular pulse with $V'_i = V'_{i,\max}$.

The dependence of the drain capacitance C_d on the drain voltage V_h and drain current I_d contributes an error that can be evaluated from the charge partition as worst case:

$$V_{e,C_d} \approx -V_{hp} \frac{C_d}{C_h} \approx -V_{hp} \frac{C_{ox}WL}{C_h} \left(\frac{1}{3} + \xi \right) \quad (6)$$

where we assumed $C_h \gg C_d$ and ξ is a coefficient related to the drain to bulk capacitance typically

about 1/3 for sub- μm CMOS technologies. The voltage and current dependence of ξ makes this error contribution somewhat non-linear. Eq. (6) is a conservative upper limit, which assumes that C_d changes from $\approx 100\%$ to $\approx 25\%$ of its full value (the drain overlap capacitance does not change) in proximity of the peak. After Eq. (2) and for a maximum V_{hp} equal to V_{DD} , it follows as the maximum error:

$$V_{e,C_d} \approx -V_{DD} \frac{2V'_{i,\max}L^2}{\mu_p(V_{DD} - V_T)^2} \left(\frac{1}{3} + \frac{1}{3} \right). \quad (7)$$

In Fig. 3, the single contributions $V_{e,C_{gd}}$, $V_{e,Q_{ch}}$, and V_{e,C_d} are shown, in absolute value and normalized to V_{DD} , as functions of $V'_{i,\max}$ for a 0.35 μm CMOS technology with $V_{DD} = 3.3\text{ V}$, $V_T = 0.8\text{ V}$, $\mu_p = 0.013\text{ m}^2/\text{V s}$. From the figure, we see that a $> 70\text{ dB}$ accuracy can be easily achieved even for rail-to-rail triangular pulses with peaking time of some tens of ns. It is worth noting that, because the contributions may be of different sign, some cancellation can occur.

For pulses with finite peak curvature, as in the semi-Gaussian case, the contributions are smaller than those predicted by Eqs. (4), (5) and (7). In the limiting case of a peak curvature approaching zero, $V_{e,C_{gd}}$ is attenuated by a factor V_T/V_{DD} ($\delta V_g = V_T$) while both errors V_{e,C_d} and $V_{e,Q_{ch}}$ approach zero.

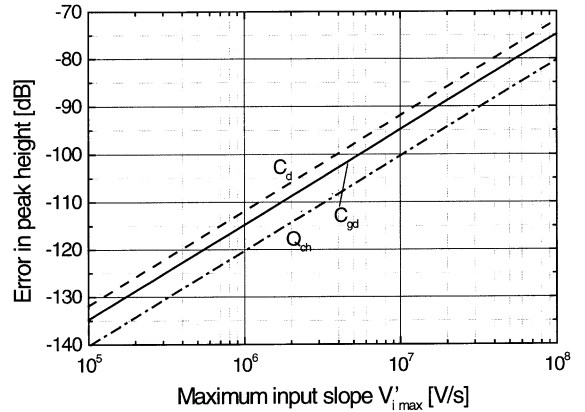


Fig. 3. Error in peak height due to M_1 , normalized to V_{DD} .

2.2.2. Errors due to amplifier A

The amplifier A introduces errors through the finite DC gain A_0 , the finite DC common mode rejection ratio (CMRR), the common mode output reference $V_{o,cm}$, the input offset V_{off} , the input-to-input capacitive coupling C_c , the dependence of the input capacitance C_i on the input voltages V_i^+ and V_i^- , and the finite speed of A (see Fig. 4). The first four parameters (A_0 , CMRR, $V_{o,cm}$, and V_{off}) contribute an error $V_{e,DC}$, which can be evaluated from Fig. 4 as follows:

$$V_{o,cm} + A_0(V_h - V_{off}(V_i) - V_i) + \frac{A_0}{\text{CMRR}} \frac{V_h + V_i - V_{DD}}{2} \approx V_{gp} \quad (8)$$

where $V_{o,cm}$ is the common mode output reference for $V_i^+ = V_i^- = V_{DD}/2$, V_{gp} is the gate voltage in proximity of the peak and we put in evidence that the offset can be voltage-dependent (e.g. rail-to-rail input configurations for low voltage supply). By approximating in Eq. (8), $V_h + V_i \approx 2V_i$ and by solving for $V_{e,DC} = V_h - V_i$, we obtain

$$V_{e,DC} \approx \frac{V_{gp} - V_{o,cm}}{A_0} + V_{off} - \frac{1}{\text{CMRR}} \frac{2V_i - V_{DD}}{2}. \quad (9)$$

For very large values of A_0 and CMRR, the error $V_{e,DC}$ turns out to be limited by the offset voltage V_{off} . This voltage is related to the mismatch between the input MOSFETs of the input differential stage. For a $0.35 \mu\text{m}$ CMOS technology with $L_i = 0.4 \mu\text{m}$, and assuming a minimum offset layout (i.e. common centroid), the standard deviation of V_{off} , expressed in rms volts, is given

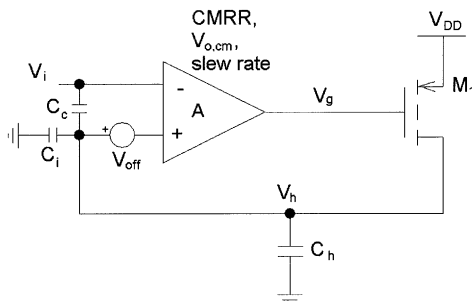


Fig. 4. Schematic of the PDH showing sources of error from amplifier A.

by

$$V_{off} \approx \frac{A_{vt}}{\sqrt{W_i L_i}} \quad (10)$$

where A_{vt} is a coefficient which depends on the technology ($\approx 8 \times 10^{-9} \text{ V m}$ in our case [10]). In Fig. 5, the normalized error V_{off}/V_{DD} is shown as function of the gate width W_i for $L_i = 0.4 \mu\text{m}$. It can be seen that in order to achieve a $>60 \text{ dB}$ accuracy, the value of W_i must be at least $10 \mu\text{m}$.

After the peak has been detected, the fast negative-going edge of the pulse (with amplitude δV_i) is present at the inverting input of A. This edge is coupled to the hold node through C_c , where it contributes an error

$$V_{e,C_c} \approx \delta V_i \frac{C_c}{C_h} \approx \delta V_i \frac{C_{ox} W_i L_i}{C_h} \frac{1}{2} \left(\frac{2}{3} + \eta \right). \quad (11)$$

In Eq. (11), we assumed an input differential stage for A, with W_i and L_i being, respectively, the gate width and length of the input MOSFETs, $C_h \gg C_c \approx C_{ox} W_i L_i (2/3 + \eta)/2$. Assuming the worst case of a transition $\delta V_i = V_{DD}$ and $\eta = 1/5$ it follows from Eq. (11) that

$$V_{e,C_c} \approx V_{DD} \frac{C_{ox} W_i L_i}{C_h} \frac{1}{2} \left(\frac{2}{3} + \frac{1}{5} \right). \quad (12)$$

The dependence of the input capacitance C_i on the input voltages V_i^+ and V_i^- contributes an error, which can be evaluated from the charge partition for a maximum $V_{hp} = V_{DD}$, by considering that

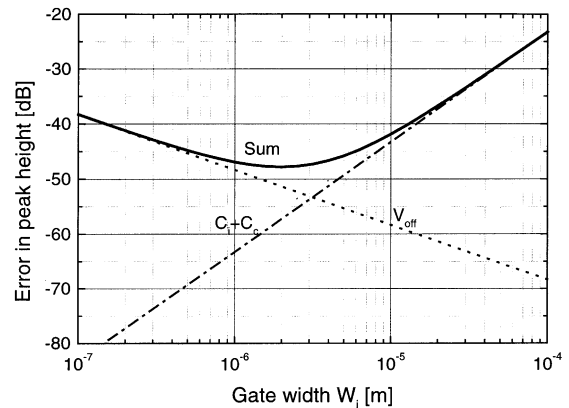


Fig. 5. Normalized error in peak height due to amplifier input capacitance and offset, as a function of input transistor gate width. In this simulation $L_i = 0.4 \mu\text{m}$ and $C_h = 2 \text{ pF}$.

the input MOSFET enters the linear region and that the overlap capacitance does not change:

$$V_{e,C_i} \approx V_{hp} \frac{C_i}{C_h} \approx V_{DD} \frac{C_{ox} W_i L_i}{C_h} \frac{1}{3}. \quad (13)$$

In Fig. 5, the total input coupling error $V_{e,C_a} = V_{e,C_c} + V_{e,C_i}$ normalized to V_{DD} is shown as a function of the gate width W_i , for $C_h = 2$ pF and $L_i = 0.4$ μm . In order to achieve a > 60 dB accuracy, the gate width W_i must be < 2 μm . Since this requirement conflicts with the one for minimizing the error due to offset (see Eq. (12)), a compromise between the two should be adopted. The result of this compromise (see Fig. 5) shows that even if relatively large values for C_h are used, a 60 dB accuracy is no more achievable. The introduction of an input series switch that opens once the peak is detected may partially attenuate the contribution due to C_c .

The finite speed of A contributes an additional error $V_{e,a}$ that should be calculated by solving the following non-linear differential equation:

$$C_h V'_h = I_D(V_h, V_g(V_h, V_i)) \quad (14)$$

where the function $I_D(V_h, V_g)$ models the MOSFET M_1 and it is non-linear, and the function $V_g(V_h, V_i)$ models the amplifier A and, for the stability issues discussed later in this section, it may also be non-linear. A worst case approximation of the error $V_{e,a}$ can be obtained by assuming a triangular pulse with rise slope $V'_i = V'_{i,max}$ and zero fall time. Once in proximity of the peak, the gate signal must perform a worst case transition from 0 to V_{DD} . If the output stage of A is slew rate limited to $V'_{g,max}$, the time required to switch M_1 off is $(V_{DD} - V_T)/V'_{g,max}$. The hold signal V_h consequently exhibits a worst case error:

$$V_{e,a} \approx - \frac{V'_i}{V'_{g,max}} (V_{DD} - V_T). \quad (15)$$

In Fig. 6, the accuracy $V_{e,a}/V_{DD}$ as function of $V'_{i,max}$ for a reasonable value of $V'_{g,max} = 10^{10}$ V/s is shown. In the same figure, the contribution $V_{e,DC}$ from Eq. (9) (case $V_{o,cm} = V_{DD} - V_T$, $V_{off} = 0$, $CMRR = \infty$ and $A_0 = 10^3$) and the sum of both, in absolute value and normalized to V_{DD} , are also shown. Due to the opposite signs of contribution (16), cancellation occurs in this case for

$V'_{i,max} \approx 10^7$ V/s. From Fig. 6, it can also be observed how the contribution $V_{e,a}$ may compensate part of the contribution $V_{e,DC}$. In Fig. 7, a simulated detail around the 3.3 V peak of the triangular pulse for the two limiting cases of Fig. 6 is shown (the contribution $V_{e,DC}$ may resemble a delay). Again, for pulses with finite peak curvature, as in the semi-Gaussian case, the contribution $V_{e,a}$ is smaller than that predicted by Eq. (15). In the limiting case of a peak curvature approaching zero, $V_{e,a}$ also approaches zero.

In summary, the accuracy of the classic CMOS PDH of Fig. 1 is limited by static and dynamic errors arising from the non-idealities of the

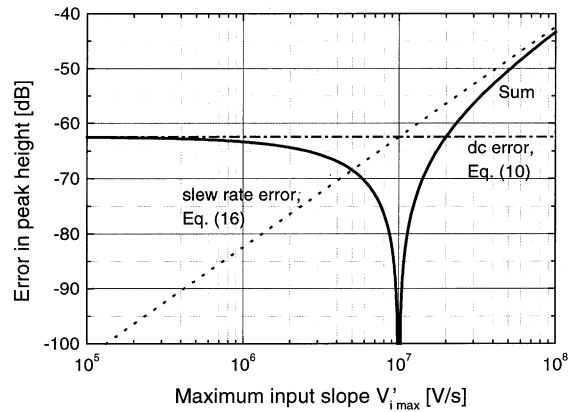


Fig. 6. Normalized errors due to finite slew rate (Eq. 14) and input mismatch (Eq. 8). Due to the different sign of the two contributions, cancellation occurs in this case for $V'_{i,max} \approx 10^7$ V/s.

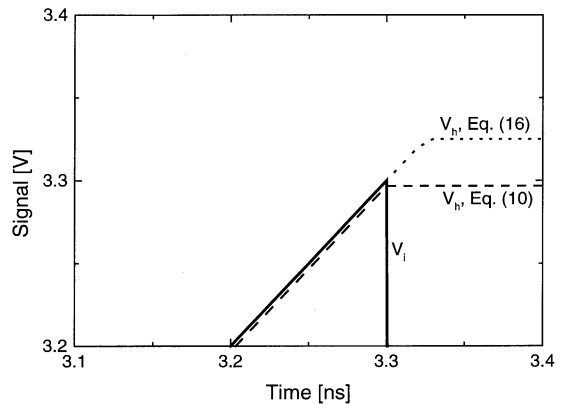


Fig. 7. Simulation of the detail around the 3.3 V peak of a triangular pulse for the two limiting cases of Fig. 6.

rectifying current source and the error amplifier. A total of ten error sources have been considered in this section and approximate expressions for their contributions are given in Eqs. (4), (5), (7), (9), (12), (13) and (15). The most important static error source is the amplifier offset. Dynamic errors are more serious for fast input waveforms with abrupt transitions.

2.3. Stability analysis

2.3.1. Simple PDH

Due to the finite bandwidth of A, the configuration shown in Fig. 1 may exhibit, in the track state, a critically damped or even unstable response. In Fig. 8, a PSpice simulation of an underdamped response for the case $A(s) = 10^3 / (1 + s \times 10^{-7})$, $C_h = 1$ pF and $W/L = 2 \mu\text{m} / 0.4 \mu\text{m}$ is shown. Clearly, ringing of the hold node will degrade the accuracy of the PDH.

The stability in the track state can be investigated by evaluating the small-signal transfer function $F(s) = V_h(s) / V_i(s)$ from the schematic of Fig. 9. In the figure, the MOSFET M_1 is represented by a simplified equivalent circuit (g_m, r_o) and the amplifier is approximated as having a single pole response. Hence, the PDH behaves as a two-pole system, with one pole at ω_a contributed by the amplifier and another at ω_h associated with M_1 and the hold capacitor C_h . The small-signal parameters g_m and r_o depend on V_g (i.e. depend on V_i').

In the tracking state, the transfer function changes with V_i depending on its slope V_i' . To each value of V_i' correspond specific values of the transconductance g_m and output resistance r_o of M_1 . The maximum value of g_m and minimum value of r_o are achieved when V_i' reaches its maximum. The time constant $\tau_h = C_h r_o$, reaches its minimum. Conversely, the minimum value of g_m and maximum value of r_o are achieved when V_i' reaches its minimum (i.e. in proximity with the peak). The time constant τ_h , reaches its maximum and, indeed, approaches an infinite value. The pole ω_h is consequently the dominant pole of the loop at this time. In order to avoid an underdamped response, it becomes necessary, but not sufficient, that the pole ω_h remains dominant during all the

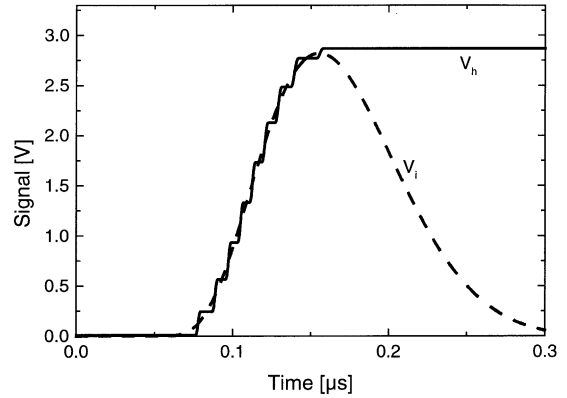


Fig. 8. PSpice simulation of an underdamped response of the PDH to a semi-Gaussian pulse.

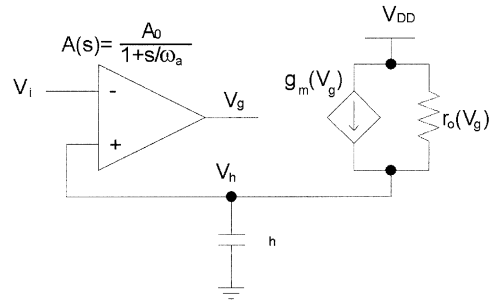


Fig. 9. Simplified schematic of the PDH for evaluating the stability of the loop.

tracking, even when ω_h reaches its maximum value (i.e. when the slope V_i' reaches its maximum), which means: $\omega_h \ll \omega_a$ during all tracking. This leads to a constraint on the gain-bandwidth product (GBW) of the amplifier (see Appendix A):

$$GBW \geq \frac{4A_0^2 V_{i\max}'}{\pi(V_D - V_T)} \tag{16}$$

The condition (16) can impose unfeasible values on the GBW of the amplifier when reasonable values of $A_0 (> 10^3)$ are used and fast pulses need to be processed. For instance, in order to handle 500 ns pulses and maintain an error of $< 0.1\%$ ($A_0 > 10^3$), the amplifier needs a gain-bandwidth product in the THz range.

Techniques for stabilizing the loop in order to increase the speed of the classical PDH were widely investigated in the past [11,12]. Placing a cascode stage in series with M_1 , together with a

current generator parallel to M_1 to minimize the changes in g_m does not improve the stability; the net result is to increase the DC loop gain and to shift of the dominant pole to a lower frequency. Moreover, an additional parasitic pole at the source of the cascode is added to the loop.

2.3.2. Lead-lag compensation

Another solution consists of a resistor R_h in series with C_h as shown in Fig. 10. The net result is to introduce a zero in the loop gain, thus effectively improving the stability. The condition for the stability leads to (see Appendix B)

$$R_h > \frac{4}{\omega_a C_h}. \quad (17)$$

On the other hand, the signal V_C (see Fig. 10) is subject to a first-order low-pass filtering (time constant $C_h R_h$) with respect to the tracking signal V_h . The value stored in C_h is consequently the value of $V_h(t)$ at $t \approx t_{pk} + C_h R_h$, with an attenuation with respect to the peak of V_h of the order of $V'_{i\max} C_h R_h$ (limiting case).

In Fig. 11, a simulation under the same conditions of Fig. 8 but with $R_h = 10 \text{ k}\Omega$ is shown. Now the response is properly damped, but the stored peak is subject to the described error. Even if this additional error is linear, its dependence on R_h and on the curvature of the peak suggests its minimization, which corresponds to the condition

$$R_h < \frac{\varepsilon V_{DD}}{C_h V'_{i\max}} \quad (18)$$

where ε^{-1} is the relative peak height accuracy required (i.e. 10^{-3} for a 60 dB accuracy). The condition (18) strongly limits R_h down to values that may conflict with the stability condition (19). For instance, in order to handle 500 ns pulses and maintain an error of $<0.1\%$ ($A_0 > 10^3$) with a $\text{GBW} \approx 10 \text{ GHz}$, the condition (16) leads to $C_h R_h > 0.64 \times 10^{-7} \text{ s}$ while the condition (17) leads to $C_h R_h < 0.5 \times 10^{-9} \text{ s}$. As a design criterion, the maximum value of R_h that satisfies the condition (18) should be used, being also aware that additional compensation techniques may probably be required to avoid an underdamped response.

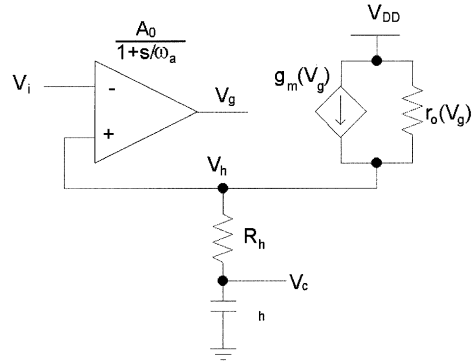


Fig. 10. Schematic of the PDH stabilized by the addition of series resistor R_h .

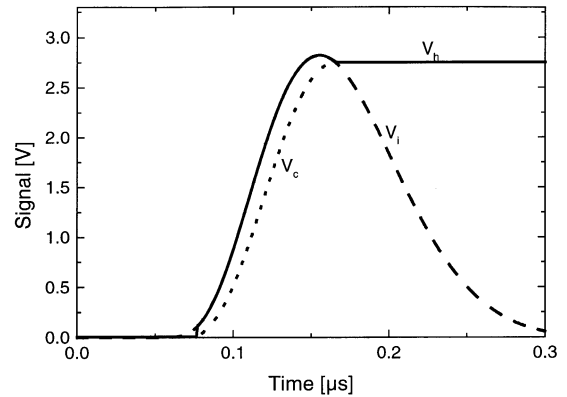


Fig. 11. PSpice simulation of a properly damped response of the PDH as in Fig. 10 to a semi-Gaussian pulse.

2.3.3. Current-mirror compensation

The current-mirror-like compensation technique, suggested by Kruiskamp and Leenaerts in 1994, is the last and most effective to this aim, and can be combined with lead-lag compensation to achieve a properly damped PDH. The configuration originally proposed by Kruiskamp and Leenaerts [1], is shown schematically in Fig. 12. It uses a current mirror, M_g-M_1 , as the rectifying element. The current mirror is driven by an operational transconductance amplifier (OTA) G_0 , which serves the same purpose as the error amplifier A in Fig. 1. The stability of this configuration is easier to achieve when compared to the simple PDH of Fig. 9, because the dominant pole

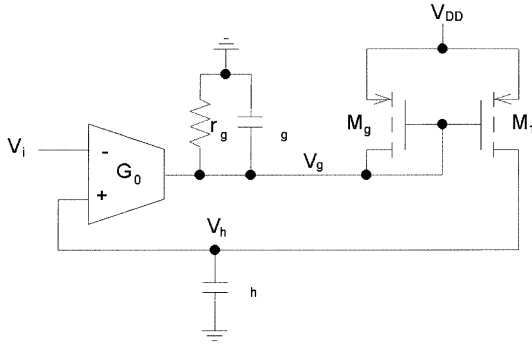


Fig. 12. Schematic of the PDH stabilized through the current-mirror.

of the amplifier ω_a varies with the input slew rate V'_i in the same way as the dominant pole ω_h . When V'_i increases during tracking, the transconductance of M_g increases, raising the pole frequency ω_a at the same time, as the dominant pole ω_h is also increasing due to increasing g_m .

In Appendix C, the stability analysis of this configuration is reported. It is also shown how the condition for a properly damped system leads to a minimum value for the gate width W_g of M_g (Eq. C.8) and to a corresponding maximum value for the voltage gain $A_{0,max} = G_0 r_g$ (Eq. C.9), depending on the maximum input slope V'_{imax} and on the value of the parasitic capacitance C_{gp} at the output of the OTA. For instance, in order to handle 100 ns pulses with $C_{gp} \approx 100$ fF, a minimum $W_g \approx 20 \mu m$ is required for $A_0 = 10^4$, and a maximum value of $A_0 \approx 5 \times 10^4$ is allowed.

Due to its effectiveness and versatility, the solution of Fig. 12 will be adopted as state-of-the-art for the stabilization of the classical CMOS PHD. The condition on $A_{0,max}$ can be further relaxed if the compensation resistor R_h , as shown in Fig. 10 and previously discussed, is added.

2.4. Driving capability

Some type of buffer must be used in order to read out the hold capacitor without disturbing the stored peak value V_{hp} . If an out-of-loop buffer is introduced as shown in Fig. 13a, an additional non-negligible error may be introduced due to

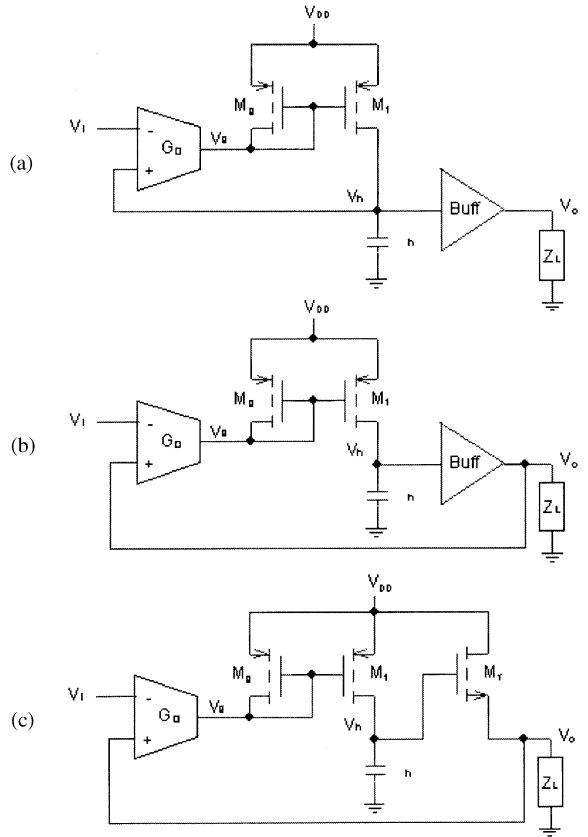


Fig. 13. Buffering techniques to provide driving capability to the classical PDH: (a) buffer outside the loop; (b) buffer in the loop; (c) source follower in the loop.

non-ideality of the buffer (finite open-loop gain, finite CMRR, voltage-dependent offset, non-linearity, etc.) and switching activity of multiplexing when the buffer is shared by more than one PDH. If an in-loop buffer is introduced as shown in Fig. 13b, the effect of the non-ideality of the buffer is minimized, at a cost of further design effort to stabilize the loop and additional area and power if multiplexing occurs.

A widely used technique to provide driving capability with minimum area, power dissipation and impact on the loop stability is a MOSFET source follower M_f as shown in Fig. 13c, where for simplicity, we omitted the current source for M_f . This solution has two major drawbacks. First, the overall dynamic range decreases by an amount

equal to the threshold voltage V_T of M_f . This impact is important in sub- μm technologies where V_{DD} is limited to a few times V_T . Second, the gain of the follower depends on the load when the loop is open, and the impact may be relevant if the PDH is heavily loaded, as in driving a highly multiplexed bus.

2.5. The current state-of-the-art configuration

In Fig. 14, the complete schematic proposed by Kruskamp and Leenaerts in 1994 and adopted and improved by other research groups [6–8] is shown. It is the opinion of the authors that this configuration represents the current state-of-the-art in CMOS PDH circuits. The OTA is realized by a differential stage, and a MOSFET switch M_{rst} is added for resetting the hold node. From the previous analysis, the following major limitations apply to this configuration:

- OTA limited in DC gain A_0 and CMRR, with consequent impact on the accuracy according to the first and third terms of Eq. (9).
- OTA characterized by high values of V_{off} (mismatch between input MOSFETs M_a and M_b and asymmetry of the differential stage), with consequent impact on the accuracy according to the second term of Eq. (9). It also forces the choice of gate widths W_i towards larger values as shown in Fig. 5.
- OTA characterized by high values of C_i and C_c (from previous constraint), with consequent

impact on the accuracy according to Eqs. (12) and (13).

- OTA limited in input common mode range due to the threshold voltage of M_a and M_b and saturation voltage of I_i , with consequent inability to process pulses of absolute amplitude below $(V_{DD} - V_T - V_{dsat})$.
- OTA limited in output dynamic range due to the saturation of M_a with consequent inability to drive gate voltages V_g below $(V_i - V_T + V_{dsat})$. Eq. (1) must be modified forcing the choice of a larger size for M_1 with consequent impact on the accuracy according to Eqs. (3), (5) and (6). The negative impact on the equations for the stability must also be considered (see Section 2.3).
- Dynamic range limits make this circuit less useful in scaled CMOS with low supply voltage.
- PDH limited in driving capability due to M_f as discussed in Section 2.4.

Results have been reported from an improved version of this configuration operating at very low power [6]. For slow pulses (10 μs peaking time), an excellent linearity ($<0.1\%$) was demonstrated, but with an overall dynamic range limited to $V_{DD}/2$ and pedestals up to several tens of mV.

3. Conclusions

Classical CMOS PDH circuits have been analyzed. They have found widespread application

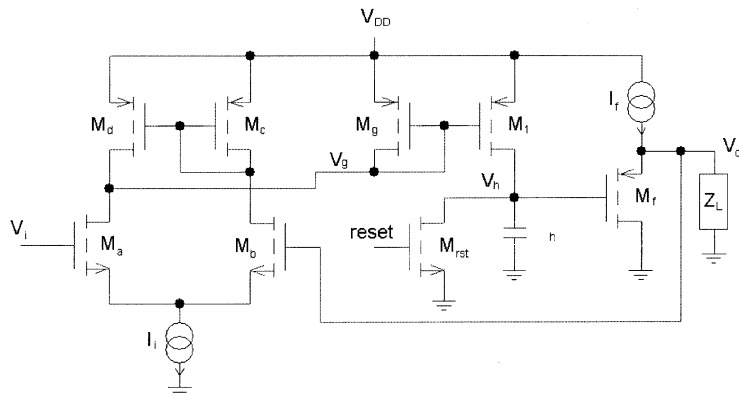


Fig. 14. Complete schematic of the PDH proposed by Kruskamp and Leenaerts in 1994.

and we have tried to understand their limits before making a further step in their development. The major error sources, stability and driving capability were analyzed. It was shown that, due to offset and capacitive coupling, the *absolute* accuracy achievable by the classical configuration is limited to the percent range. The same limits apply to the configuration, which represents the current state-of-the-art in CMOS PDH.

A novel two-phase approach, which overcomes the major limits was consequently developed. We report on this configuration in a related paper (Part 2).

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Appendix A

Under the assumption $A_0 g_m r_o \gg 1$, the transfer function $F(s) = V_h(s)/V_i(s)$ can be approximated:

$$F(s) = \frac{V_h(s)}{V_i(s)} \approx \frac{1}{s^2 \frac{1}{\omega_h \omega_a A_0 g_m r_o} + s \frac{\omega_h + \omega_a}{\omega_h \omega_a A_0 g_m r_o} + 1}. \quad (\text{A.1})$$

The damping factor δ can be easily calculated and approximated as

$$\delta = \frac{\omega_h + \omega_a}{2\sqrt{\omega_h \omega_a A_0 g_m r_o}} \approx \frac{1}{2} \sqrt{\frac{\omega_a C_h}{A_0 g_m}}. \quad (\text{A.2})$$

The maximum value $g_{m,\max}$ of g_m which corresponds to the maximum expected slope $V'_{i,\max}$ can be evaluated by differentiating Eq. (2) with respect to V_g and by imposing $V_g = 0$:

$$g_{m,\max} = \mu_p C_{ox} \frac{W}{L} (V_{DD} - V_T) = \frac{2C_h V'_{i,\max}}{V_{DD} - V_T}. \quad (\text{A.3})$$

The minimum value δ_{\min} of δ turns out to be

$$\delta_{\min} \approx \frac{1}{2} \sqrt{\frac{\omega_a C_h}{A_0 g_{m,\max}}} = \frac{1}{2\sqrt{2}} \sqrt{\frac{\omega_a (V_{DD} - V_T)}{A_0 V'_{i,\max}}}. \quad (\text{A.4})$$

The system is properly damped when $\delta_{\min} \geq 1$, i.e. when

$$\frac{A_0}{\omega_a} \geq \frac{1}{8} \frac{V_D - V_T}{V'_{i,\max}} \quad (\text{A.5})$$

which translates into Eq. (17) by considering that $2\pi G_{bwp} = A_0 \omega_a$.

Appendix B

The transfer function $F(s)$ becomes

$$F(s) = \frac{V_h(s)}{V_i(s)} \approx \frac{1 + s\gamma/\omega_h}{s^2 \frac{1}{\omega_h \omega_a A_0 g_m r_o} + s \frac{\omega_h + \omega_a(1 + \gamma A_0 g_m r_o)}{\omega_h \omega_a A_0 g_m r_o} + 1} \quad (\text{B.1})$$

where $\gamma = R_h/r_o$. The damping factor δ_{\min} can be easily calculated and approximated assuming $\gamma \ll 1$:

$$\delta_{\min} \approx \frac{1}{2} \sqrt{\frac{\omega_a C_h}{A_0 g_{m,\max}}} (1 + A_0 g_{m,\max} R) \quad (\text{B.2})$$

which suggests that, in order for R_h to be effective, $A_0 g_{m,\max} R_h \gg 1$ should be satisfied. For a properly damped system, this leads to Eq. (18).

Appendix C

The OTA is characterized by a transconductance DC gain G_0 and by a dominant pole located at the output node with time constant:

$$\frac{1}{\omega_a} = \frac{C_g r_g}{1 + r_g g_{m,g}} \quad (\text{C.1})$$

where C_g is the total output capacitance, r_g the (ideally infinite) OTA output resistance and $g_{m,g}$ is the transconductance of M_g . With this approach, the DC voltage gain A_0 from the differential input to the gate of M_1 turns out to be

$$A_0 = \frac{G_0 r_g}{1 + r_g g_{m,g}}. \quad (\text{C.2})$$

By replacing A_0 and ω_a from Eqs. (C.1) and (C.2) into Eq. (A.2), the damping factor δ becomes

$$\delta \approx \frac{1}{2} \sqrt{\frac{C_h(1+r_g g_m)^2}{C_g G_0 r_g^2 g_m}} \approx \frac{1}{2} \sqrt{\frac{C_h(1+\lambda r_g g_m)^2}{C_g A_{0,\max} r_g g_m}} \quad (\text{C.3})$$

where λ is the ratio between W_g of M_g and W of M_1 ($L_g = L$ is required for matching reasons), and $A_{0,\max}$ is the maximum DC voltage gain, achieved in proximity of the peak where g_m approaches zero. Eq. (C.3) has a minimum δ_{\min} for $r_g g_m = \lambda^{-1}$:

$$\delta_{\min} \approx \frac{1}{2} \sqrt{\frac{4\lambda C_h}{C_g A_{0,\max}}}. \quad (\text{C.4})$$

By imposing $\delta_{\min} \geq 1$, the condition on λ follows

$$\lambda \geq A_{0,\max} \frac{C_g}{C_h} \quad (\text{C.5})$$

which, by putting in evidence W_g , becomes

$$W_g \geq W A_{0,\max} \frac{C_{gp} + C_{ox} W_g L(1/3 + \eta)}{C_h}, \quad (\text{C.6})$$

where C_{gp} is the parasitic capacitance non-related to M_g and $C_g \approx C_{gp} + C_{ox} W_g L(1/3 + \eta)$. Solving condition (C.6) for W_g the following results:

$$W_g \geq \frac{W A_{0,\max} \frac{C_{gp}}{C_h}}{1 - A_{0,\max} \frac{C_{ox} W L}{C_h} (1/3 + \eta)} \quad (\text{C.7})$$

which, from Eq. (3) gives ($\eta = 1/5$):

$$W_g \geq \frac{A_{0,\max} \frac{2V'_{\max} L}{\mu_E (V_{DD} - V_T)^2} \frac{C_{gp}}{C_{ox}}}{1 - A_{0,\max} \frac{2V'_{\max} L^2}{\mu_P (V_{DD} - V_T)^2} (1/3 + 1/5)} \quad (\text{C.8})$$

effective until

$$A_{0,\max} < \frac{\mu_P (V_D - V_T)^2}{2V'_{\max} L^2} \frac{1}{(1/3 + 1/5)}. \quad (\text{C.9})$$

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