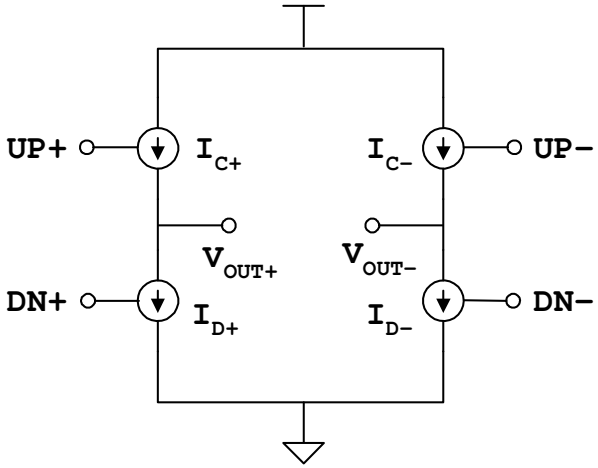
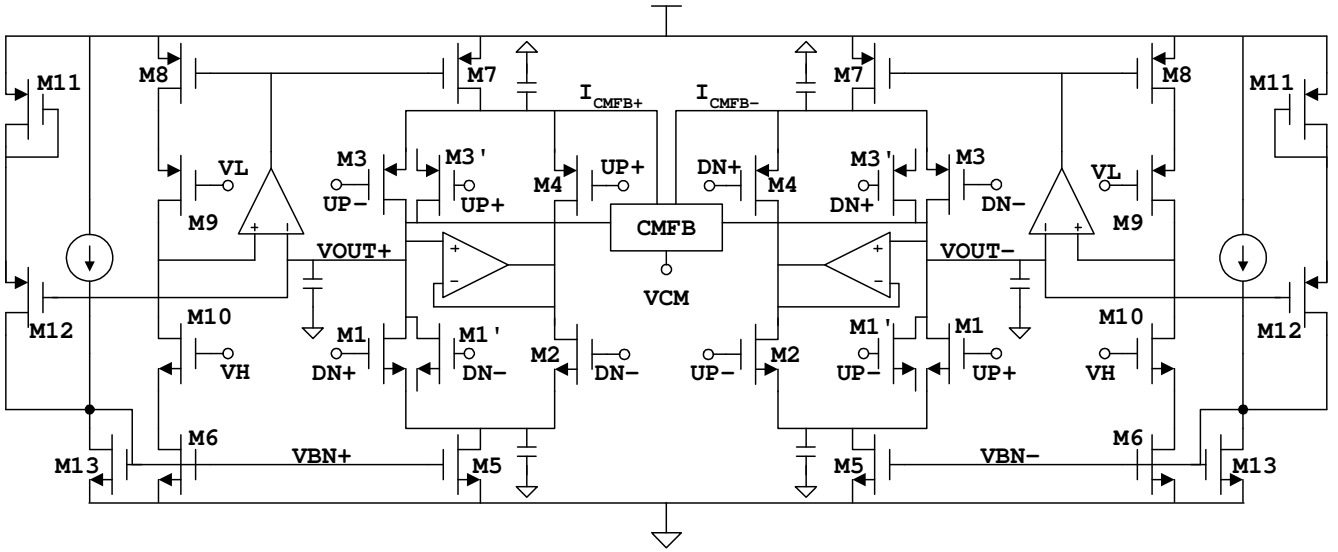
"Design and Analysis of an Ultrahigh-Speed Glitch-Free Fully Differential Charge Pump with Minimum Output Current Variation and Accurate Matching,"

S. Cheng, H. Tong, J. Silva-Martinez and A. Karsilayan, IEEE Transactions on Circuits and Systems, part II, Vol. 53, pp. 843 - 847, Sept. 2006

Simple? Complex?





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An ultrahigh-speed fully differential charge pump with minimum current mismatch and variation is proposed in this paper.

A mismatch suppression circuit is employed to minimize the mismatch between the charging and discharging currents, which minimizes the steady-state phase error in a Phase-Locked Loop (PLL).

A variation suppression circuit is proposed to minimize output current variation with the change of output voltage, which reduces the variation of the bandwidth in a PLL.

Techniques are proposed to suppress both low-speed glitches and high-speed glitches to allow glitch-free operation of the charge pump with ultra-fast input pulses.

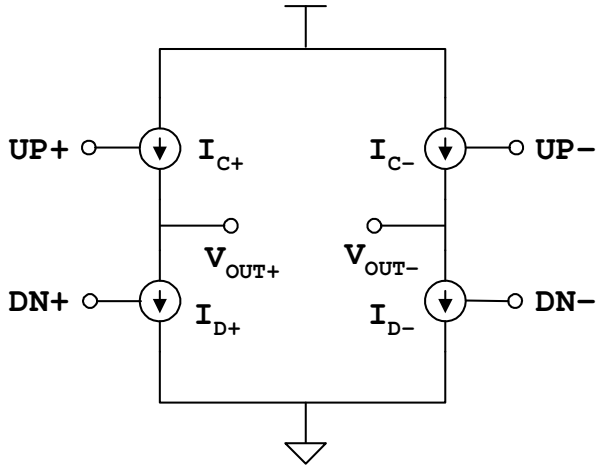
ACCURATE MATCHING AND MINIMUM CURRENT VARIATION

Existing solutions use a common mode feedback to control the outputs.

The common mode feedback, however, cannot eliminate the differential error caused by the mismatch between charging and discharging current when the differential output voltage is not zero.

To illustrate this issue, let us define the output voltages as

$$V_{OUT+} = V_{CM} + \Delta V \; ; \quad V_{OUT-} = V_{CM} - \Delta V \qquad (1)$$



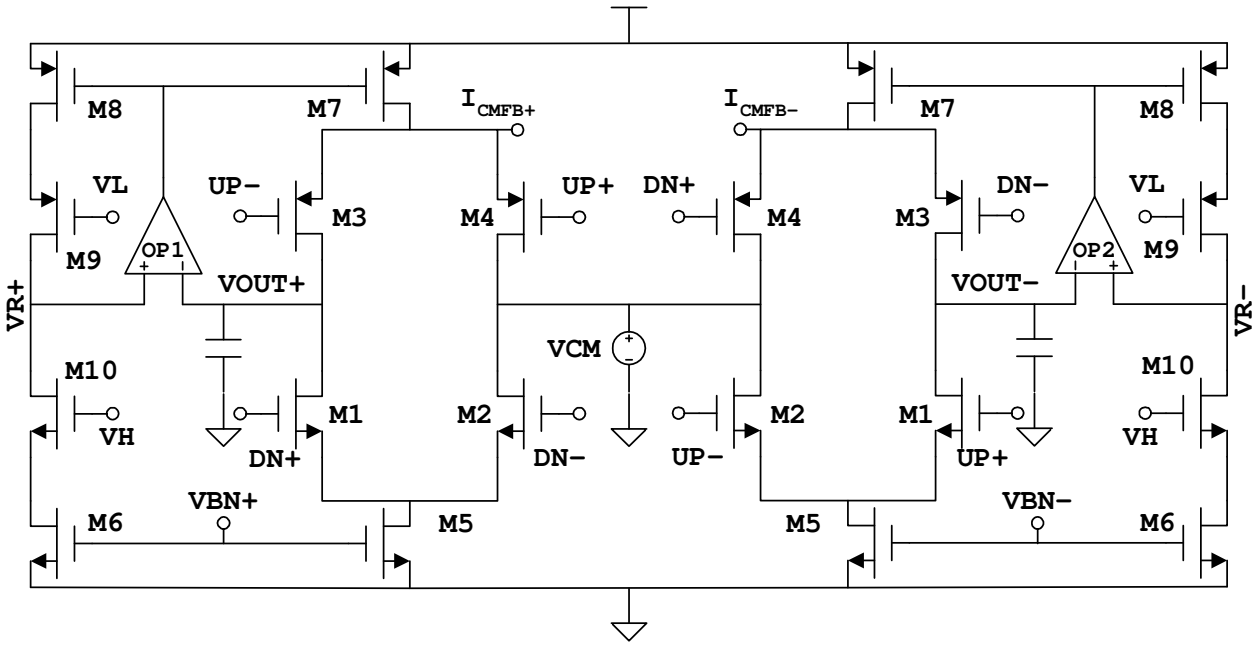
Due to the channel length modulation effect, the charging current will be smaller than the discharging current on the positive output terminal while the charging current will be larger than the discharging current on the other side.

$$I_{C+} = I_{D-} = I_0 - \Delta I \; ; \quad I_{C-} = I_{D+} = I_0 + \Delta I \qquad (2)$$

The overall differential output current as,

$$I_{diff} = (I_{C+} - I_{D+}) - (I_{C-} - I_{D-}) = -4\Delta I \qquad (3)$$

This error cannot be corrected by the common mode feedback circuit since the two output voltages are symmetric around the common mode level. Thus, the PLL will settle to a non-zero phase error.



Differential charge pump with excellent mismatch suppression.

The terminals I_{CMFB+} and I_{CMFB-} are reserved for injection of common mode feedback current.

Two opamps are used to ensure that $V_{R+} \cong V_{out+}$ and $V_{R-} \cong V_{out-}$. The amplifiers force the charging current to follow the discharging current exactly.

VH and VL are the logic low level and logic high level of the differential input signal.

The discharging current flowing through M1 is equal to the current flowing through M10 because the

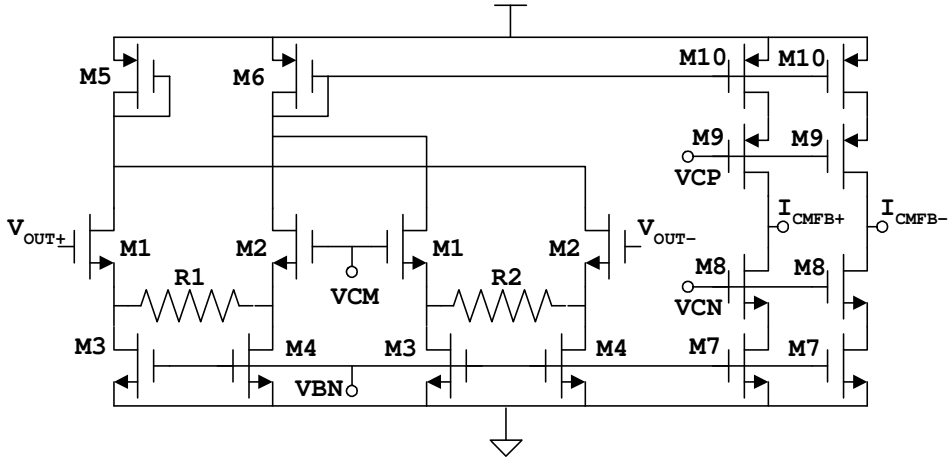
transistor pairs (M1, M5) and (M10, M6) are matched in both size and bias.

The opamp used in this design is a simple one-stage opamp with moderate gain for compensate.

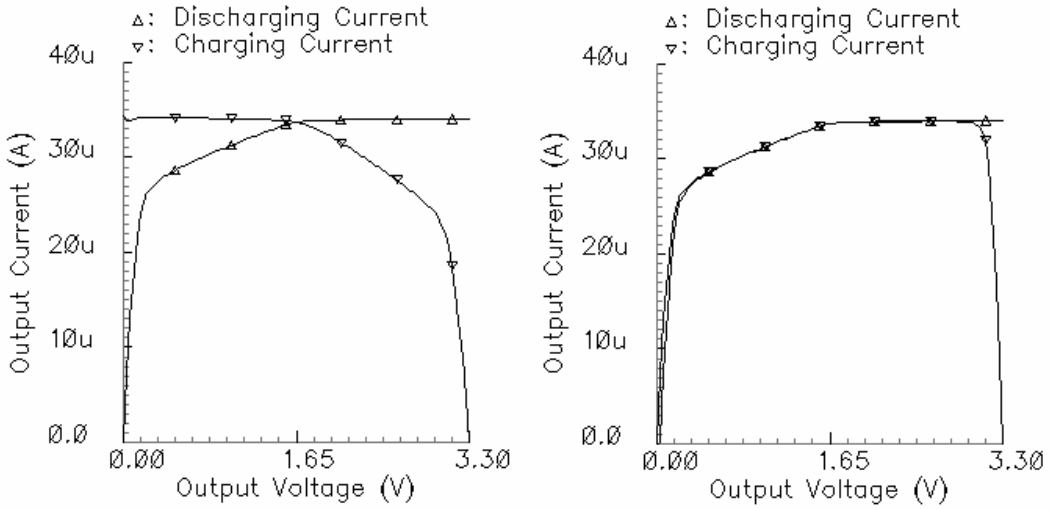
A relatively large capacitor must be added to properly compensate the feedback loop and ensure stability.

The common mode feedback circuit used amplifies the common mode error signal and converts it into two output currents with the same value.

Resistive source degeneration is used at the input stage to maximize the linear input swing so that the common mode feedback circuit can work properly over a large voltage range.



Common mode feedback circuit for the charge pump.



(a) Without mismatch suppression **(b) With mismatch suppression**

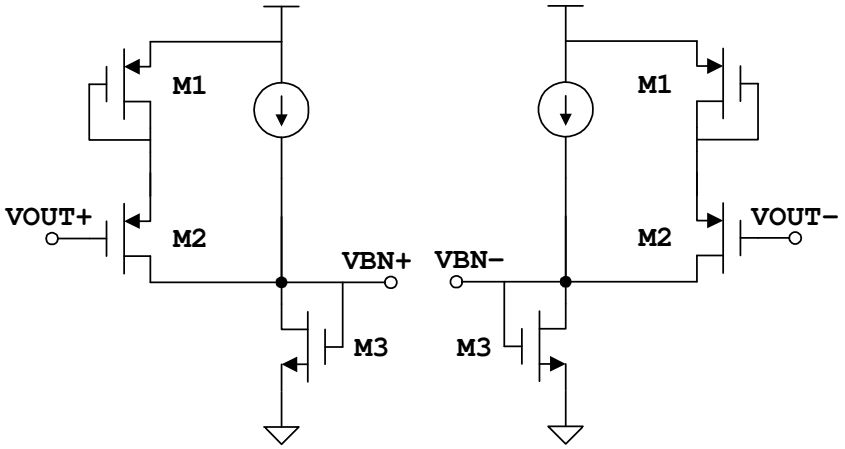
Output currents with and without mismatch suppression.

Suppression of Output Current Variation

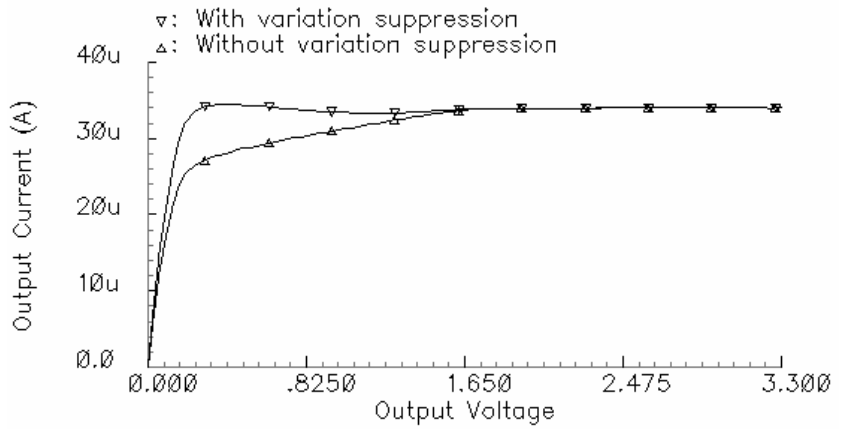
It is evident in previous circuit, both output currents decrease when the output voltage goes towards the ground level.

Variation of charge pump output current results in variation of the loop bandwidth that may bring the PLL from a stable region to an unstable region.

To suppress the current variation dependent on the output voltage, we propose to dynamically adjust the bias voltages $V_{BN\pm}$ and hence the charge pump bias current.



Variation suppression circuit.



Charge pump current with and without variation suppression.

When the output voltage goes low enough to push the NMOS output transistor into triode region, M1-M2 from the compensation circuit starts to conduct and injects current into M3. That results in an increase of the bias current for the charge pump as an effective compensation.

As a rule of thumb, M2 can be designed to conduct when the output transistor starts to enter triode region, i.e., $V_{OUT}=2V_{dsat,NMOS}$. DC sweep simulation can be done to achieve optimum compensation in actual design.

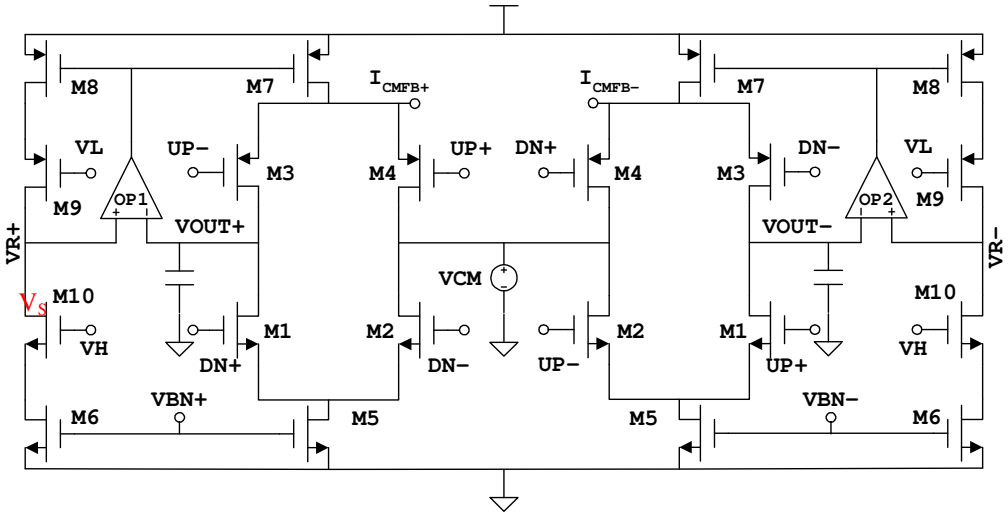
Variation suppression technique extends significantly the range of the output voltage for a given variation tolerance. The output current variation is controlled within 3% when the output voltage is higher than 0.2V.

Glitch Suppression

The output current pulse has glitches whose magnitude increases with the speed of the input signal.

A. Low-Speed Glitch

The first type of glitch is caused by the speed-limitation of the common source node of the differential pairs.

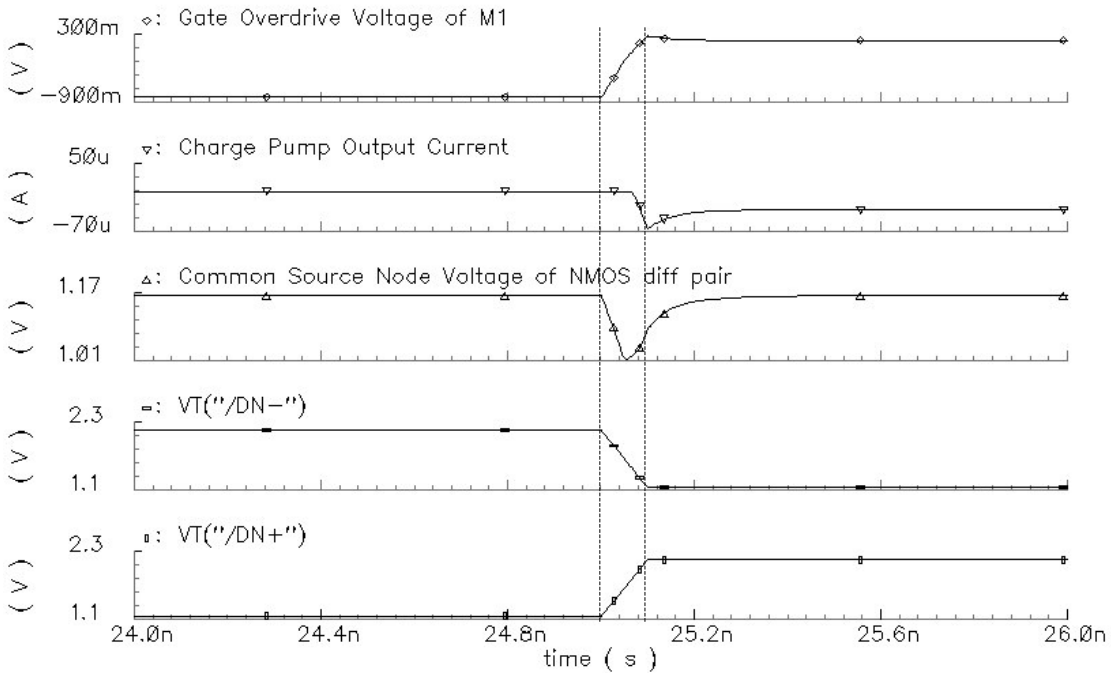


When the input is balanced, V_S is equal to $V_{S1}=V_{CM}-V_{TH}-V_{dsat,M1}$.

When the differential pair is fully switched to one side, it can be shown that V_S is equal to $V_{S2}=V_H-V_{TH}-\sqrt{2}\,V_{dsat,M1}$,

Thus, with slow input pulse, V_S goes down to V_{S1} when the input is balanced and goes back to V_{S2} when the input is fully switched to the other side.

However, when the input signal is very fast, V_S is not able to settle to the value of V_{S2} as soon as the input finishes switching, due to heavy parasitics at the common source node.



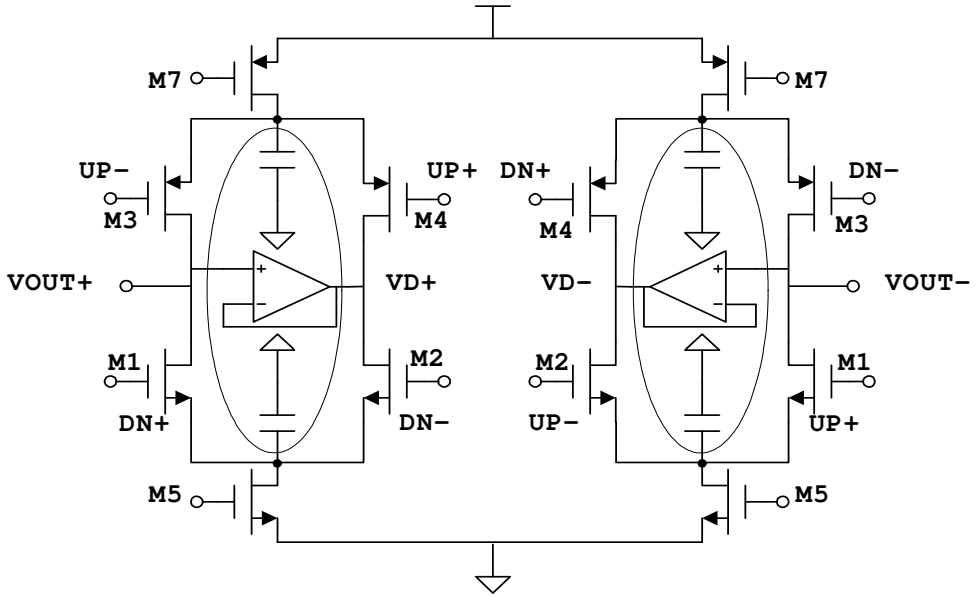
The circuit shown in below minimizes the low-speed glitches.

Two relatively large capacitors are added at the common source nodes of the differential pairs. They are used to minimize the voltage variation on the common source nodes during the transition of the input signal by pulling the common source node down to a much lower speed compared with the input signal.

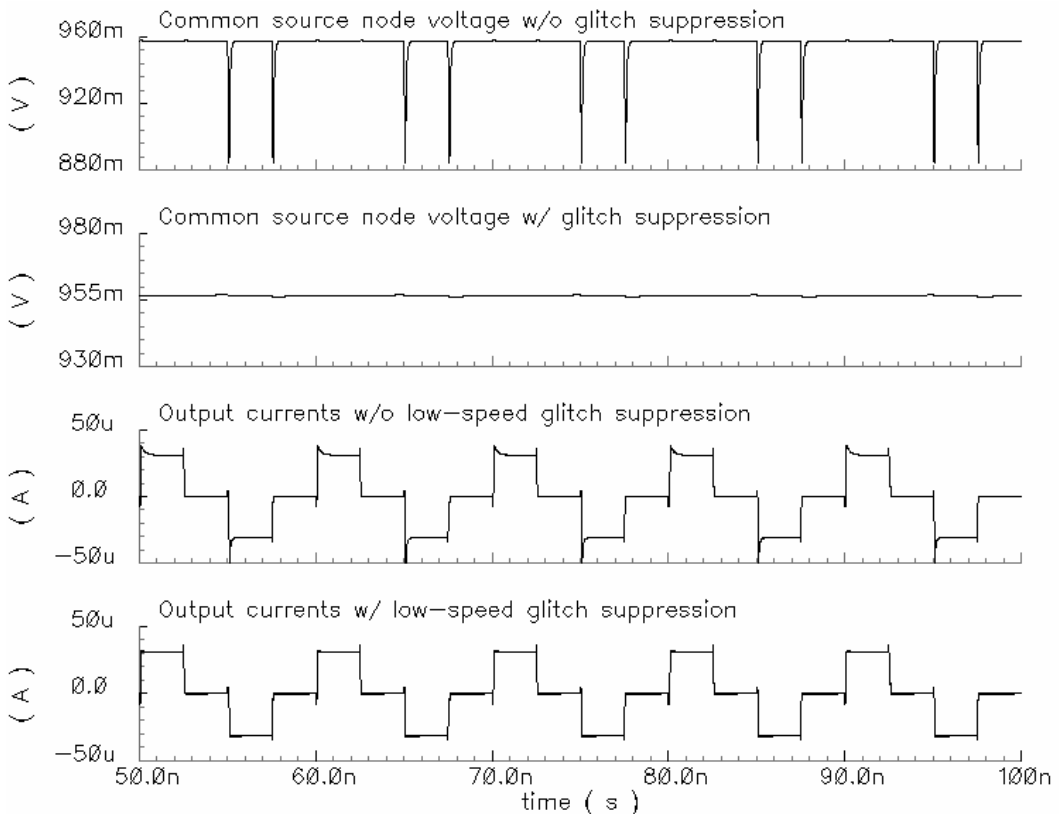
Also, instead of using a fixed bias for V_D, an amplifier in unity-gain feedback configuration is added to

ensure that V_{out} and V_D have very close voltages. As a result, the common source node will have the same voltage before and after the switching.

The actual value and size of the capacitors depends on the slew rate of the input signal, the capacitor value added at the common source node is about 0.5pF. When the transition time is hundreds of picoseconds, we could need a capacitor value up to 5pF.



Charge pump with low-speed glitch suppression circuit.



Common source node voltage of NMOS diff. pair and output current with and without low-speed glitch suppression circuit.

High-Speed Glitch

The high-speed glitch is generated by charging or discharging the gate-to-drain capacitance (C_{gd}) of the output transistors, which directly injects current into the output node.

The generated glitch current is expressed below,

$$I_{glitch}=C_{gd}(V_H-V_L)/\Delta T=C_{gd}K$$

where K represents the slew rate of the input voltage during transition.

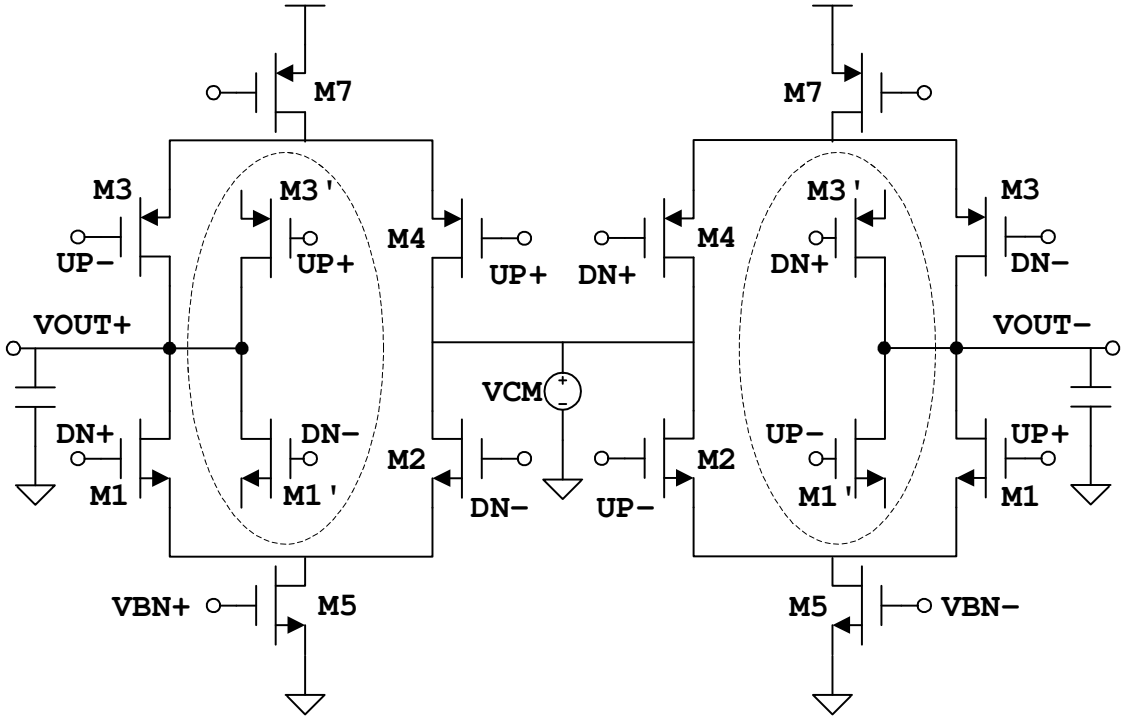
This kind of glitch is very narrow and has approximately the same width as the input transition time.

If somehow the output transistor goes into deep triode region (e.g., the NMOS output transistor will go into triode region when the output voltage is very low), C_{gd} will be close to half the MOS gate capacitance, i.e.,

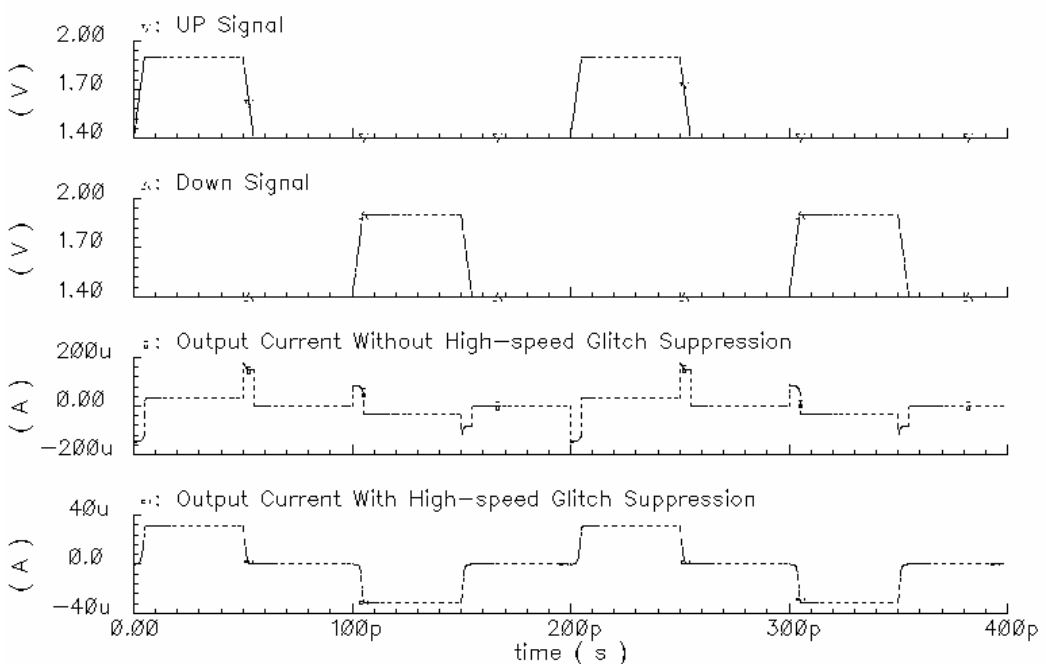
$$C_{gd}=C_{gs}=C_{gg}/2=WLC_{ox}/2$$

When this happens, the gate-to-drain capacitance will be several times larger and so is the induced glitch current.

To minimize the glitch, it's always desirable to keep the output transistors in saturation region. Even more, it maximizes the switching speed of the charge pump if the output transistors work in saturation region instead of triode region.

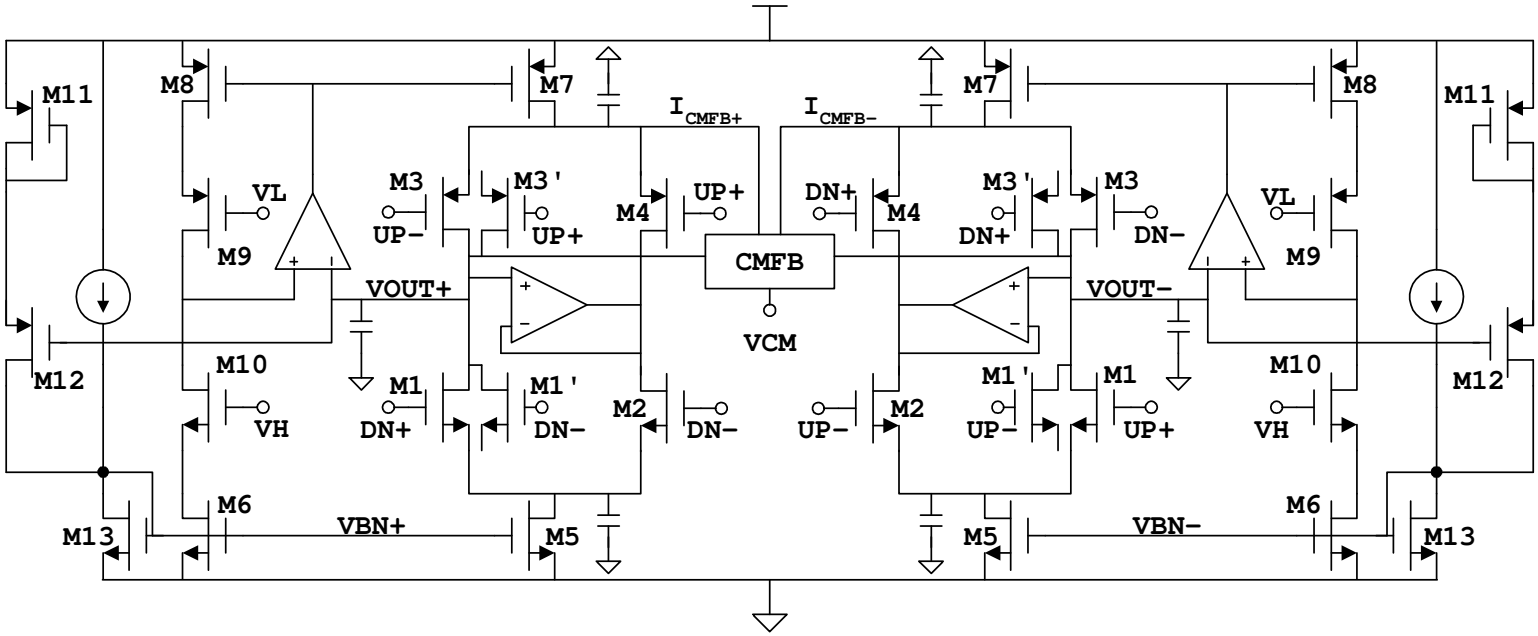


Charge pump with high-speed glitch suppression circuit using dummy devices (enclosed in ellipses).



Output current with and without suppression of high-speed glitch.

Complete schematic of the fully differential charge pump employing all the techniques discussed in the previous sub-sections



Complete schematic of the proposed charge pump.

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[10] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York: McGraw-Hill, 2001, chapter 15, pp. 550-556

[11] J.-S. Lee, M.-S. Keel, et al., “Charge pump with perfect current matching characteristics in phase-locked loops”, *Electronics Letters*, vol. 36, pp. 1907-1908, Nov. 2000.

[12] I.A.Young, J.K.Greason, et al., “A PLL clock generator with 5 to 10 MHz of lock range for microprocessors”, *IEEE Journal of Solid State Circuits,* vol. 27, pp. 1599-1607, Nov. 1992.

Response to reviewer #1:

Thanks for all the helpful comments.

(1)A first point to note is the following. In most charge pumps, devices M1 to M4 are operated as switches (thus, they operate either in the cut-off or in the triode region). As, in the proposed scheme, these devices are operated in saturation, it should be better to provide some words to underline the reason for this choice.

As indicated in the paragraph enclosing equation (5), one reason that the input transistors are preferred to operate in saturation region is that the transistors have smaller gate-to-drain capacitance in saturation. Another reason is that the transistors can switch at a faster speed in saturation region than in triode region. These comments were added to the end of that paragraph to clarify the issue.

(2)The issue of low-glitches seems to be not so clear. The paper states that the problem of glitches is due to the presence of an excessive gate-to-source voltage when the gate voltage of one of the devices in the differential pair, i.e., M1 and M2 (or M3 and M4) in Figure 2, rises very fast. According to the paper, referring to the NMOS differential pair, this is due to the fact that the common source of the differential pair is not able to follow the rising input signal. The technique to solve this problem consists in connecting

a (large) capacitor between the common-source node and ground. This ideally leads to a constant voltage at the common source node. We think that, if the low-speed glitch problem is due to the above cause, the presence of this capacitor should enhance rather than alleviate the problem. Indeed, the presence of this capacitor leads to a more constant voltage at the common-source node. This is also shown in the simulated waveforms in Figure 8 (in this Fig! ure, it is also not clear why the large negative glitches are present in the common-source node without the glitch suppression capacitor). Therefore, we think that the item of low-speed glitches should be explained in a more clear way.

0 is added to illustrate the generation mechanism of low-speed glitches. Detailed explanation is added into the first paragraph after the sub-title “Low-speed glitch”. The introduction of the large capacitance at the common source node is to intentionally slow down the speed so that the common source node voltage experiences little variation before and after the switching of the input signal. Thus, there is no overshoot of gate-to-source voltage and the glitches are eliminated.

(3)As for the paper organization, generally a paper is made up of more than three Sections (here, the body of the paper is included in only one Section).

Thanks for the suggestion. The body part is divided into three sections now. The first section talks about the schematic of the differential charge pump with mismatch and variation suppression, which are mainly

about DC properties. The second section talks about glitch suppression, including high-speed glitches and low-speed glitches, which are mainly about transient properties. The third section shows the complete schematic combining all the proposed techniques.

(4) The technique to ensure accurate matching of the charging and the discharging output current is basically derived by reference [9], as pointed out in the paper.

Yes, We agree with that. We basically did proper adaptation of that technique to make it suitable to be used in the fully differential charge pump. Also we emphasized the importance of differential mismatch, which is not suppressed by CMFB circuit but often overlooked by designers. We give credit to [9] in that section.

(5) The operation of the circuit proposed to minimize output voltage variation as a function of the output voltage, is rather clear in principle. However, from a design point of view, it should be interesting to know some design criteria for this circuit (which is the criterion to determine the output voltage level which causes devices M1 and M2 in Figure 5 to conduct?).

As a rule of thumb, M2 can be designed to conduct when the output transistor starts to enter triode region, i.e., $V_{OUT}=2V_{dsat,NMOS}$. DC sweep simulation can be done to achieve optimum compensation in actual design. This rough design criteria is added into the first paragraph after 0.

(6)As for the technique to minimize on high-speed glitches, are the source terminals of the dummy devices (M1 and M3 in Figure 9) floating?

Regarding the high-speed glitch suppression techniques, the source of the dummy transistors is floating because we don't want them to conduct any current to affect the output current value. In this case, there is no difference between the source and drain terminals because they have the same voltage. This is mentioned in the first paragraph after figure 11.

(7)Abstract, line 7. We think that it could be specified that the target is to minimize the variation of the output current amplitude as a function of the output voltage, rather than simply the variation of the output current amplitude.

Abstract was updated as suggested.

(8)Index terms. We think it could be better to say "current variation" rather than simply "variation".

Index terms were updated as suggested.

(9) Reference [10] is cited before reference [9] (both on page 2, left column). Therefore, we think that the numbers of these two references should be exchanged.

The order of reference [9] and [10] was exchanged as suggested.

(10) Control signals UP+, UP- look in different positions, with respect to control signals DN+ and DN-, in Figure 1 and Figure 2. This is probably due to the fact that, in Figure 2, signals UP+ and UP- are applied to PMOS devices. If so, probably, this should be stated in the paper, so as to prevent any risk of misunderstanding by the reader.

Thanks for pointing out the potential confusion. We have added brief explanation in the passage (WHAT DO YOU MEAN? BE MORE ESPECIFIC) below 0 to indicate the fact that both UP and DN signal are active at high level.

(11) Page 3, right column, line 7 from bottom of the column. We think that "unit-gain" could be replaced by "unity-gain".

"Unit-gain" was changed to "Unity-gain" as suggested.

(12) Figure 7. We think that, to avoid any risk of misunderstanding, the drain node of M4 and M2 should not be labeled as VR+ and VR-, as these labels are also used for other nodes in Figure 2.

We have renamed “VR” in 0 and related text into “VD” to avoid confusion with 0.

(13) Caption to Figure 7 and to Figure 9. Probably, “ellipses” could be better than “eclipses”.

Thanks for pointing out the typos. They were corrected in the caption of 0 and 0.

(14) Figure 8. It should be better to specify that the first two waveforms are referred to the common source of the NMOS differential pair. Also, the corresponding waveforms of signals DN+ and DN- could be shown, to help the reader for better understanding.

The caption of 0 was revised to indicate that the common source node voltage refers to the NMOS differential pair. For the waveforms of DN+ and DN-, please refer to 0 which is newly added.

(15) Page 5, first line. We think that “PMOS devices” could be more appropriate than “PMOS”.

“PMOS” was changed into “PMOS devices” as suggested.

(16) Page 5, left column, line 10. Probably, "drawn" could be better than "drowned".

??? Changed "drown" into "corrupted" in Page 5, left column, line 15.

(17) Equation (6). It could be better to replace VCM with another label, as label VCM is used in Figures 2 and 11.

The V_{CM} in 0 and Equation (6) means the same thing, i.e., the desired common mode bias voltage, usually $V_{DD}/2$. Thus we think it might be proper to use the same label for consistency.

(18) Equation (7). Probably, VTH-NMOS and VTH-PMOS are exchanged

Thanks for pointing out the typo. It was corrected as suggested.

(19) Page 5, left column, line 3 from bottom of this column. We think that this line should begin with "The".

"The" was added at the beginning of the second paragraph of page 5 as suggested.

Response to reviewer #2:

Thanks for all the helpful comments.

(1) Give the reference to the book of D. Leenaerts & oth "Circuit design for RF Transceivers", Kluwer 2001. This book explains very well (in Ch. 7) the detrimental effects of the charge pumps (in nondifferential form) that you are discussing.

Thanks for suggesting the reference. It was added as reference [6] in the paper.

(2) Explain or give the reference to the schematic of operational amplifiers that you are using. You are claiming the results for transistor level simulation, yet the schematic of OPAmps is not given.

Explanation for the opamp used in this design was added with proper reference at the end of the first paragraph after 0. In actual design, the gain of the opamp depends on the accuracy requirement. A rail-to-rail input stage can be added to maximize the accurately-matched output swing of the charge pump if necessary.

(3) Misprint: page 5, second column, line 10 from top. Should be small "t", not capital.

We couldn't find the mentioned error in page 5. We found a similar mistake in page 4 instead. Thus we guess there is a typo in the comment. We changed "e.g., The NMOS output transistor" to "e.g., the NMOS output transistor" in page 4 according to the suggestions.

(4) It is a good simulation work. Unfortunately, there is no realization.

Thanks for the comment. We are planning to fabricate a CDR using all these techniques. Since the chip design, fabrication and testing of the entire CDR will take a while, we would like to publish these ideas as soon as possible.

Response to reviewer #3:

Thanks for all the helpful comments.

(1) First, this ideas are good, but there are something to be verified in the real application

Thanks for the comment. We are planning to fabricate a CDR using all these techniques. Since the chip design, fabrication and testing of the entire CDR will take a while we would like to publish these ideas as soon as possible.

(2) The minimum output current variation is a good point. However, a well designed PLL will operate to decrease that kind of nonlinear effect.

The proposed suppression technique minimizes the output current variation from the aspect of charge pump design. Meanwhile, a well-designed PLL does have to have tolerance for the variation of the charge pump current due to additional process variation, as pointed by the reviewer. However, minimizing the current variation in charge pump design can provide larger margin on the system-level design of a PLL.

(3) When this charge pump is applied in the wireless communication, this proposed one needs 4 opamp and several current source. Thus, the circuit needs the very high power consumption. Did you check power consumption?

The opamps used in this design don't need a high bandwidth. It need only be faster than the voltage stored in the large loop filter capacitor. That is, the unity-gain bandwidth of the opamp just need larger than the loop bandwidth of the PLL, which is usually no more than a few MHz. What's more, the opamp doesn't have to drive large capacitance as catalog opamp products do. Thus, the opamps used in this charge pump consume relatively small power. Give a value of power used in the charge pump and a typical power used by VCOs and prescaler.

(4) The capacitance will be helpful to reduce the the glitch level in Fig 7. However, it is dangerous thing to add capacitor, because it will be considered as an unexpected pole. Moveover maximum total capacitance is 20pF, too large size. MOS capacitor is not good for precise matching and large process variation.

The large capacitor added on the common source node only decreases the common mode rejection ratio at high frequencies to some extent. However, it doesn't affect the frequency response and stability for

differential signal. MOS capacitor can be used because the exact capacitor value and its linearity are not so critical in this particular application.

(5) The additional mos pairs are used to reduce glitch in this paper. The small capacitor size can be used to achieve same function by proper Mos size as Equation (5). Did you check the difference?

Theoretically, a small linear capacitor of the same value can be used to cancel the high-speed glitches. However, there is no way to ensure accurate matching between a linear capacitor (e.g., a metal-to-metal capacitor) and the gate-to-drain capacitor of a MOS transistor. Thus, we choose to use dummy MOS transistors to produce well-matched coupling capacitance.

(6) To verify this idea, I would like to ask author that performance improvement in whole loop, not just single unit including power consumption and real speed.

DO some macromodel simulation for the entire PLL with the typical PLL and your charge pump, and compare jitter and spurs. Report just the values of the comparison.