DETAILED FREQUENCY ANALYSIS OF POWER SUPPLY REJECTION IN BROKAW BANDGAP

G. Giustolisi, G. Palumbo

DEES - Università di Catania
V.le A. Doria, 6
I-95125, Catania, Italy
e-mail: ggiustolisi@dees.unict.it, gpalumbo@dees.unict.it

ABSTRACT

A detailed frequency analysis of Power Supply Rejection (*PSR*) in Brokaw bandgap voltage reference is carried out. The knowledge of the frequency behavior in a voltage reference becomes mandatory to the designer especially in RF or digital environment where disturbs coming from supply lines becomes more evident. Precise and simple models, useful for pencil and paper analysis, are developed and a compensation technique for improving the circuit frequency performance is also discussed. Results are validated by comparing the carried-out models with the actual circuit by means of SPECTRE.

1. INTRODUCTION

Since its introduction, the Brokaw bandgap reference [1] (or an equivalent version [5]) has been widely used in a wide range of applications such as A/D and D/A converters, voltage regulators, measurements, instrumentation circuits, etc. The bandgap reference generates a dc voltage that is ideally temperature independent. This is achieved by adding a voltage, which is proportional to the absolute temperature (PTAT), to a base-emitter voltage in order to compensate for its first-order temperature dependency [2-3]. In the literature, performance of bandgap references has been expressed in terms of relative temperature dependency, accuracy, output impedance, power consumption, and noise [4-10]. An important parameter, such as power-supply rejection (*PSR*), and its frequency behavior, has not been already treated explicitly, although this feature becomes a fundamental design criterion in high performance applications (as instance, RF circuits and digital processing) [11]. Indeed, due to the reduction of the loop gain with frequency, spurious signals coming from the power supply could not be adequately rejected and this problem becomes more evident in RF or digital environment where disturbs due to coupled lines or to substrate noise arise. In these environments, a detailed knowledge of the bandgap frequency behavior is mandatory to the designer in order to better understand the possibilities and the main limitations of the used voltage reference.

In this communication, a detailed frequency analysis of the *PSR* in the Brokaw bandgap voltage reference is carried out and a simple and useful compensation technique to improve frequency performance is also given. For both the uncompensated circuit and the compensated one, two frequency models, which are in excellent agreement with simulations on the actual circuit, are carried out.

2. CIRCUIT ANALYSIS

2.1 Bandgap analysis

The Brokaw bandgap voltage reference is shown in Fig. 1. As well known, neglecting the base currents, the mirror sets I_{C1} equal to I_{C2}, so that the dc output voltage, V_{REF}, can be expressed by

$$V_{REF} = V_{BE1} + 2R_1 I_{C1,2} \tag{1}$$

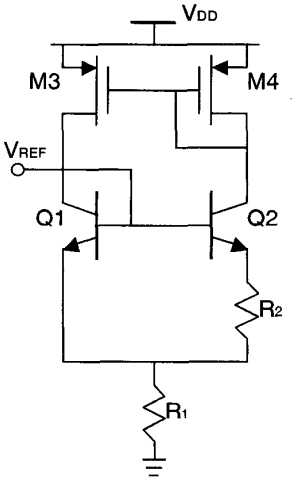

Figure 1. Brokaw bandgap voltage reference.

The drop voltage across R_2 sets the current I_{C2}, which is proportional to $\Delta V_{BE1,2}$, that is

$$I_{C1,2} = \frac{U_T}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right) \tag{2}$$

where A_{E1} and A_{E2} are the emitter areas of transistors Q1 and Q2, respectively and U_T is the thermal voltage ($U_T \cong 26\text{mV}$ @ 27°C). Substituting (2) in (1) we get

$$V_{REF} = V_{BE1} + 2U_T \frac{R_1}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right) \tag{3}$$

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$$PSR(s) \cong \frac{r_{d3} \parallel \left(\frac{k}{2} r_{c2}\right)}{R_1} \cdot \frac{1 + \frac{C_G}{g_{m1,2} g_{m3,4}} \left(1 + \frac{1}{k}\right) s + \frac{R_1}{g_{m3,4}} C_G \left[C_{db3} + C_{cs1} + C_{\mu 2}\left(1 + \frac{2}{k}\right)\right] s^2}{1 + \left[r_{d3} \parallel \left(\frac{2}{k} r_{c2}\right)\right]\left[2C_{\mu 2} + \left(1 + \frac{2}{k} C_{cs2}\right)\right] s + \left[r_{d3} \parallel \left(\frac{2}{k} r_{c2}\right)\right] \frac{C_G C_{\mu 2}}{g_{m3,4}} \left(1 + \frac{2}{k}\right) s^2} \tag{7}$$

A proper choice of transistor areas and of both R_1 and R_2 will minimize the temperature coefficient and will set the output voltage to a stable value near 1.2 V.

2.2 *PSR* model

The *PSR* can be defined as

$$PSR = \frac{1}{A_{dd}} \tag{4}$$

where

$$A_{dd} = \frac{v_{ref}}{v_{dd}} \tag{5}$$

represents the small signal gain between the output node of the bandgap and the power supply line.

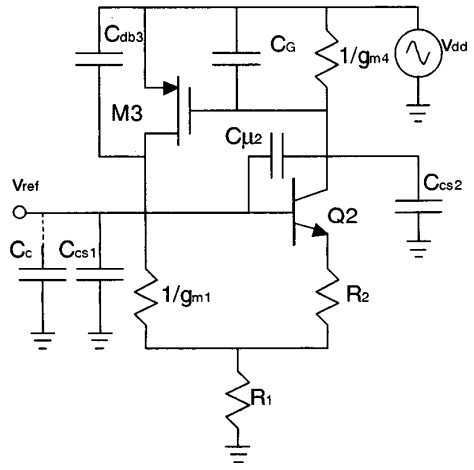

Figure 2. Small signal model of the Brokaw bandgap voltage reference.

The model used to determine the *PSR* is shown in Fig. 2. Diode connected transistors are approximated with resistors given by their transconductance. Capacitor C_G takes into account the capacitive amount between the gate of M3-M4 and the supply line and is equal to $2C_{gs3,4} + C_{db4}$. Capacitors $C_{\mu 1}$, $C_{\pi 1}$ and $C_{gd3,4}$ can be ignored because of their small value and, despite its large value (the emitter area of Q2 is larger than Q1's, usually 8 times), capacitor $C_{\pi 2}$ can be ignored too. In fact, applying the Miller theorem to $C_{\pi 2}$ and assuming in a rough approximation that Q2 acts as a voltage follower, its contribution can be demonstrated to be negligible.

Defining k as

$$k = g_{m1,2} R_2 = \ln\left(\frac{A_{E2}}{A_{E1}}\right) \tag{6}$$

a symbolic analysis yields the expression in (7) for the *PSR* where non-dominant terms have been neglected.

A fairly good approximation of poles and zeroes included in (7) can be found by evaluating the polynomial coefficient ratios [12-13], yielding

$$p_1 = -\frac{1}{\left[r_{d3} \parallel \left(\frac{k}{2} r_{c2}\right)\right]\left[2C_{\mu 2} + \left(1 + \frac{2}{k} C_{cs2}\right)\right]} \tag{8a}$$

$$p_2 = -\frac{g_{m3,4}}{C_G}\left(\frac{2k}{k+2} + \frac{C_{cs2}}{C_{\mu 2}}\right) \tag{8b}$$

$$z_1 = -\frac{g_{m3,4}}{C_G\left(1 + \frac{1}{k}\right)} \tag{8c}$$

$$z_2 = -\frac{1 + \frac{1}{k}}{R_1\left[C_{db3} + C_{cs1} + C_{\mu 2}\left(1 + \frac{2}{k}\right)\right]} \tag{8d}$$

A first look at (7) shows that the *PSR* dc behavior is mainly affected by intrinsic resistances of both Q2 and M3 and by resistor R_1. This means that the dc gain mainly depends on process parameters (such as the channel length modulation factor, λ, in MOS or the early voltage, V_A, in BJT transistors) and is independent of the bias current, $I_{C1,2}$. In fact for the bandgap to work properly the voltage across R_1 must be kept constant and equal to about 0.5 V, that is R_1 must be chosen almost inversely proportional to $I_{C1,2}$. Moreover, since also both r_{d3} and r_{c2} are inversely proportional to $I_{C1,2}$, for typical technological parameters, a gain of no more than 40 dB can be hardly achieved.

As far as the ac behavior is concerned, from (8) we can notice that the first pole, p_1, gives the dominant contribution and depends on both r_{d3} and r_{c2} (as well as the dc gain) and on parasitic capacitors of Q2. A pole-zero cancellation is obtained between the second pole, p_2, and the first zero, z_1, since they are very close each other, while the last zero, z_2, gives its contribution at very high frequencies.

As a conclusion, in RF or in modern digital circuits where disturbs from coupling lines or from the switching activity

$$PSR(s) \cong \frac{r_{d3} \parallel \left(\frac{k}{2} r_{c2}\right)}{R_1} \cdot \frac{1 + R_1 C_C \left(1 + \frac{1}{k}\right) s + \frac{R_1}{g_{m3,4}} C_G C_C \left(1 + \frac{1}{k}\right) s^2}{1 + \left[r_{d3} \parallel \left(\frac{2}{k} r_{c2}\right)\right]\left[2C_{\mu 2} + \left(1 + \frac{2}{k} C_{cs2}\right)\right] s + \left[r_{d3} \parallel \left(\frac{2}{k} r_{c2}\right)\right] \frac{C_G C_{\mu 2}}{g_{m3,4}} \left(1 + \frac{2}{k}\right) s^2} \tag{9}$$

widely affect power supply lines, this bandgap appears to have poor performance if its first pole is located in a frequency in the order of a few Megahertz.

2.3 *PSR* model with frequency compensation

Better ac performances can be obtained by inserting a compensation capacitor, C_C, between the bandgap output and ground. In the same way, a symbolic analysis yields the expression in (9) for the *PSR* where non-dominant terms have been neglected. It is worth noting that the denominator of (9) is unchanged and so will be the poles, while numerator coefficients mainly depend on C_C. In particular, the poles are the same as in (8a) and (8b) while the new expressions for the zeroes are given by

$$z_1 = -\frac{1}{R_1 C_C \left(1 + \frac{1}{k}\right)} \tag{10a}$$

$$z_2 = -\frac{g_{m3,4}}{C_G} \tag{10b}$$

A pole-zero cancellation can be obtained by choosing C_C so that $p_1 = z_1$, that is

$$C_C = PSR(0) \cdot \frac{2C_{\mu 2} + C_{cs2}\left(1 + \frac{2}{k}\right)}{1 + \frac{1}{k}} \tag{11}$$

In this way, we get a flat band *PSR* over a wide range of frequencies, since the main frequency limitations are given by the pole and the zero in (8b) and (10b), respectively, very close each other. A larger value of C_C would yield to an increase in the PSR for high frequency but, on the other hand, it would increase the startup time, too, when the bandgap is switched on.

3. VALIDATION RESULTS

The circuit was simulated and results were validated by using the SPECTRE simulator and a 0.8-μm BiCMOS technology supplied by EUROPRACTICE. Npn transistors have a β_F of 90 and a maximum f_T of 8 GHz. Both n-mos and p-mos exhibit a threshold voltage of about 0.75 V and a transconductance factor of 100 μA/V^2 and 36 μA/V^2, respectively.

The supply voltage was set to 3 V with a bias current of 100 μA in each branch. Q2 emitter area was chosen 8 times Q1's. Other useful parameters are reported in Table I.

The circuit exhibit an output voltage of 1.198 V at room temperature (27 °C) and a temperature coefficient of 16.5 ppm/°C over the range –55, +125 °C. The uncompensated bandgap was compared with the *PSR* transfer function model carried out in section 2.2. Specifically, the dc gain was carried out evaluating *PSR*(0) from (7) while poles and zeroes were evaluated from (8). Table II summarize the resulting transfer function model.

TABLE I
VALUE OF CIRCUIT PARAMETERS

Parameter	Value
$(W/L)_{3,4}$	100/4
R_1	1.93 kΩ
R_2	540 Ω
C_C	22.45 pF
$g_{m1,2}$	3.86 mA/V
r_{o2}	265.1 kΩ
$C_{\mu 2}$	79.99 fF
C_{cs1}	34.65 fF
C_{cs2}	87.22 fF
$g_{m3,4}$	382.6 μA/V
r_{d3}	658.76 kΩ
$C_{gs3,4}$	571.1 fF
$C_{db3,4}$	38.55 fF

TABLE II
COEFFICIENTS OF PSR TRANSFER FUNCTION MODELS

PSR(0)	40.04 dB
Uncompensated circuit	
p_1	$-2\pi \cdot 2.47$ Mrad/s
p_2	$-2\pi \cdot 108.67$ Mrad/s
z_1	$-2\pi \cdot 34.78$ Mrad/s
z_2	$-2\pi \cdot 533.27$ Mrad/s
Compensated circuit	
p_1	$-2\pi \cdot 108.67$ Mrad/s
z_1	$-2\pi \cdot 51.50$ Mrad/s

The result of the first ac simulation is reported in Fig. 3. As expected, the circuit exhibits a dc gain of about 40 dB. The error

between the actual circuit and the model is less than 3 dB while their frequency behavior matches perfectly.

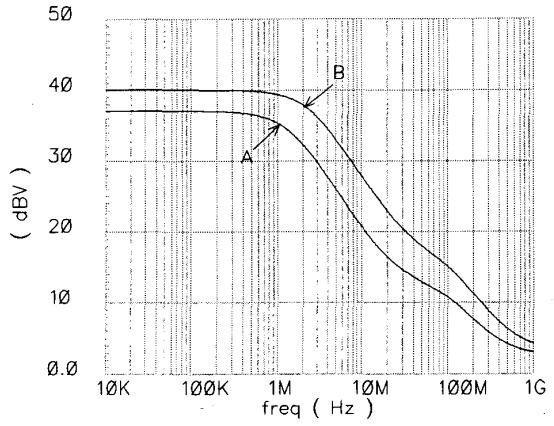

Figure 3. *PSR* vs. Frequency for circuit without compensation. A) Circuit, B) Model.

A second simulation was carried out in order to compare the compensated circuit with the model developed in section 2.3. The compensation capacitor, C_C, was chosen, according to (11), in order to obtain the pole-zero cancellation and results in 22.5 pF. The *PSR* transfer function model has the same dc gain and, due to the pole-zero cancellation, it exhibits the pole in (8b) and the zero in (10b). Their numerical values are reported in Table II.

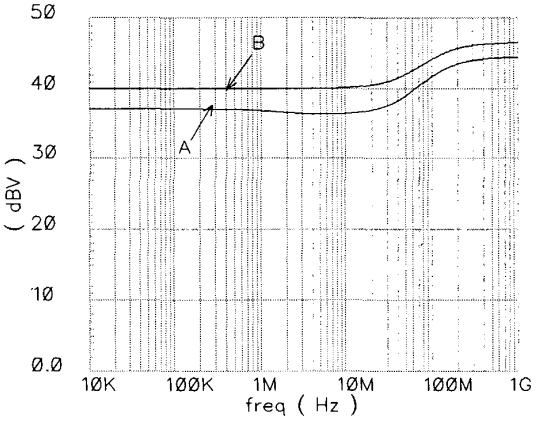

Figure 4. *PSR* vs. Frequency for circuit with compensation. A) Circuit, B) Model.

The simulation result is depicted in Fig. 4. Even in this case, the model matches with the actual circuit that exhibit a first order transfer function as expected. This result justifies also the remark in section 2.3 which suggest not increasing the value of C_C to achieve better performances at higher frequencies. In fact, it is apparent that achieving better performance would mean having a too large value of C_C that would degrade the bandgap startup time.

4. SUMMARY

In this paper the *PSR* frequency behavior of a widely used bandgap voltage reference was analyzed and a compensation technique was also carried out. Two simple models for pencil-and-paper analysis were given to the designer in order to estimate the *PSR* of the Brokaw bandgap at high frequencies. Both the compensation technique and models are useful in RF or modern digital circuits where disturbs from power supply becomes critical. Results were validated by comparing the models with the actual circuits and a good agreement is shown between simulated and expected results.

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