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Design for Test of Crystal Oscillators: A Case Study

MARINA SANTO-ZARNIK
HIPOT HYB, Trubarjeva 7, Šentjernej, Slovenia

FRANC NOVAK AND SREČKO MAČEK
Jožef Stefan Institute, Jamova 39, 1000 Ljubljana, Slovenia

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Abstract. A feasibility study of design-for-testability (DFT) of a voltage controlled crystal oscillator with built-in MOS switches to increase its observability and controllability is presented. The primary aim was to assess to what extent the operation of the circuit is changed when the switches are introduced. The possibility of non-destructive localization of faulty components in the provided test modes and the temperature/frequency characteristics measurements are briefly described. Finally, on the basis of the presented experimental work, a design-for-test procedure for crystal oscillator circuits is summarized. The work was performed in a development phase of a voltage controlled temperature compensated crystal oscillator.

Keywords: analog circuits, crystal oscillators, design-for-test, fault diagnosis

1. Introduction

The growing complexity of integrated circuits, minimization and the advent of surface-mounted device (SMD) technology make the problem of testing the assembled boards more and more difficult. Design for test (DFT) techniques are employed to keep the complexity of tests at a reasonable level.

DFT in digital domain is a mature research area with established general guidelines and well-known practical solutions [1–3], some of them even standardized, like for example IEEE standards 1149.1 and 1149.5.

On the other hand, analog DFT is still emergent [4, 5], and as noticed in [6], the general problem of DFT for analog circuits is almost certainly intractable. Hence it is more realistic to expect partial solutions suitable for specific classes of circuits. A number of such DFT solutions have recently been proposed [7–10].

In this paper we present a feasibility study of the design for test of a voltage controlled temperature compensated Pierce crystal oscillator with built-in MOS switches which are used to increase its controllability and observability. By introducing the DFT switches a circuit can be partitioned into parts that can be easily tested and fault isolation can be accomplished at the level of individual circuit components. However, an important question is if the impact of the DFT switches can be compensated so that the circuit operates within the specified tolerances. An experimental study of the impact of the DFT switches on the operation of the oscillator circuit is the main issue of this paper. The conclusions of the study are summarized in a general design-for-test procedure.

The paper is organized as follows. In Section 2, the oscillator circuit designed for testability and diagnosability is presented and the test modes corresponding to the selected switch positions are described. In Section 3, the impact of switches on the operation of the oscillator within the specified temperature range is studied and experimental results are given. The

localization of faulty passive components in the oscillator circuit is discussed in Section 4. Measurements of frequency/temperature characteristics of crystal units are described in Section 5. In Section 6, the design-for-test procedure for crystal oscillator circuits is summarized, and finally, in Section 7, concluding remarks are given.

2. DFT of Oscillator Circuit

The block diagram of a crystal oscillator can be represented as a closed loop system with an amplifier of an open-loop gain A, and a feedback network containing the crystal with a transfer function $\beta(\omega)$. In order that the circuit oscillates, the following conditions must be satisfied [11, 12]:

- the total phase shift around the closed loop must be an integer multiple of 360°,
- the loop gain at the frequency where the phase requirements are met must be greater or equal to unity.

A faulty circuit component may cause improper operation such that the circuit either does not oscillate or its frequency differs from the expected one. Since the oscillator circuit is a closed loop system, isolation of faulty components is a difficult task. The application of the design-for-test methodologies may simplify the troubleshooting and provide means for automated diagnostics.

A straightforward idea is to break the closed loop of the oscillator such that external stimuli can be applied at some external pin of the modified circuit and output observed at some other external pin. Like in [6], MOS switches can be employed for this purpose. The situation is depicted in Fig. 1. If input stimuli are applied at X_1 we can observe the response of the amplifier part of the oscillator at X_2. DC and AC responses at significant frequencies can be used in fault localization.

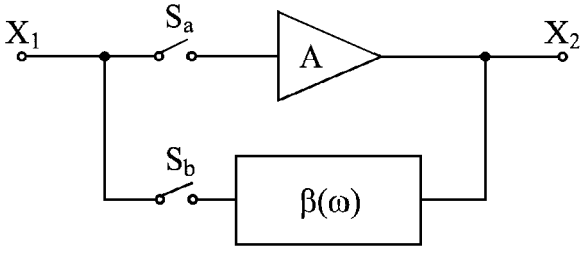

Fig. 1. Block diagram of an oscillator.

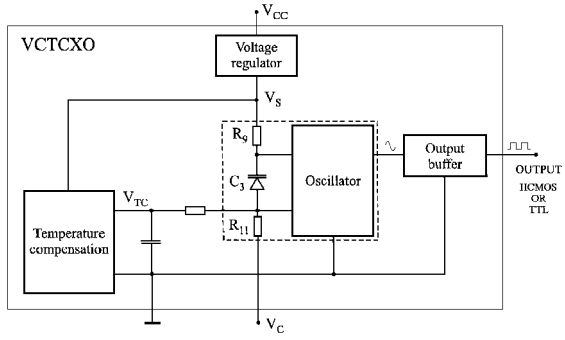

Fig. 2. Block diagram of VCTCXO.

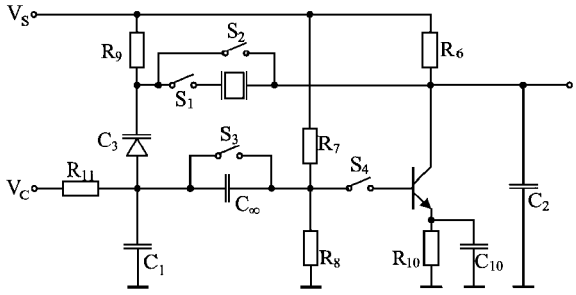

Fig. 3. Oscillator with the DFT switches.

Conversely, the feedback $\beta(\omega)$ as a passive frequency selective network and can be regarded in the frequency domain as a filter circuit. Diagnostic conclusions can be drawn from the known transfer characteristics and measured response to the known input stimuli.

The application of the above idea has been studied in a development phase of a voltage controlled temperature compensated crystal oscillator (VCTCXO) depicted in Fig. 2.

Its kernel, the Pierce crystal oscillator (presented with dashed block) is shown in detail in Fig. 3. In our case study, switches S_1, S_2, S_3 and S_4 are used to open (or short) chosen paths of the circuit. Notice that the voltage control input presented as V_c can be used in the test mode to apply stimuli to the transistor stage or to observe the response of the feedback path.

2.1. *Test Modes*

The circuit operation can be analyzed in the following modes:

- **Normal Mode:** (S_1 ON, S_2 OFF, S_3 OFF, S_4 ON), operation of the oscillator circuit is measured,

- **Test Mode 1:** (S_1 OFF, S_2 OFF), feedback cut off, analysis of the amplifier part. It comprises the following cases:
  1. (S_3 OFF, S_4 OFF), R_6 is measured at the output.
  2. (S_3 ON, S_4 OFF), values of R_7/R_8 and R_{11} are verified at the input.
  3. (S_3 ON, S_4 ON), R_6/R_{10} is determined by DC analysis. Since the value of R_6 has been measured in test mode 1 (case 1) the value of R_{10} can be verified.
     AC analysis is performed to measure operating conditions of transistor loaded by C_2.
- **Test Mode 2:** (S_1 OFF, S_2 ON, S_4 OFF), analysis of the feedback circuit, crystal unit disconnected. It comprises the following two cases:
  1. (S_3 OFF), $R_6 \parallel R_9$ is measured. Since R_6 has been verified in test mode 1, R_9 is verified.
  2. (S_3 ON), frequency characteristics of the RC feedback path is measured. Values of C_1, C_2, and C_3 are checked.

Some Further Details on Test Mode 2. The equivalent circuit of the oscillator in test mode 2 (case 2) is shown in Fig. 4. Its transition function $H(s) = V_{\text{out}}(s)/V_{\text{in}}(s)$ is given by:

$$H(S) = \frac{1}{R_{S_1'} R_{11} C_1 C_2} \cdot \frac{1}{\left(s + \frac{R_{78}+R_{11}}{C_1 R_{78} R_{11}}\right)} \cdot \frac{s}{\left(s^2 + s\frac{C_2 R_{69} + C_3 R_{69} + R_{S_1'} C_3}{R_{S_1'} C_2 C_3 R_{69}} + \frac{1}{R_{S_1'} C_2 C_3 R_{69}}\right)}$$

where R_{78} denotes $R_7 \parallel R_8$, and R_{69} denotes $R_6 \parallel R_9$. The impedance of a switch S_i, denoted by R_{S_i}, when turned ON can be modeled as a pure resistance for lower frequencies. At higher frequencies, the capacitive effect of switches in ON and OFF positions should be considered as an additional part of C_1 and C_2. Notice that since $R_{S_3} \ll R_7 \parallel R_8$, its impact is negligible and hence omitted in Fig. 4. Since in our case $R_9 \gg R_6$ and R_9, $R_6 \gg R_{S_2}$, R_6 and R_9 are presented as $R_6 \parallel R_9$.

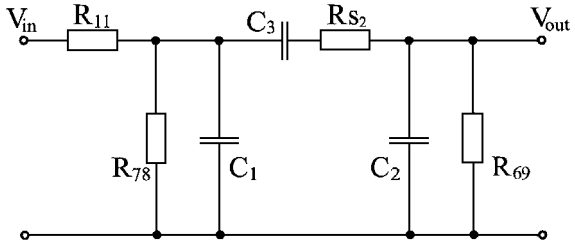

Fig. 4. Equivalent circuit in the test mode 2, case 2.

3. Analysis of the Impact of the DFT Switches

The components of the crystal oscillator circuit shown in Figs. 2 and 3, are related by:

$$3 \le \frac{g_{21}}{g_L}\frac{C_2}{C_1} \le 15$$

$$\frac{1}{C_L} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

where g_{21} is the transconductance of the transistor, g_L is the load seen by the collector and C_L is the load capacitance of the crystal. C_1, C_2, C_3 refer to the capacitances in Fig. 3.

The above gain and phase shift relations have been obtained following the approach of derivation of the Y-parameter equations for the Pierce oscillator given in [11]. The upper and lower bounds of the gain relation have been chosen in accordance with practical estimation of the overall loop gain value.

Any changes of the parameters in the above expressions obviously impact the operation of the oscillator. In the worst case the closed loop gain may decrease to the point where the circuit cannot oscillate. Otherwise if the total external capacitance to the crystal differs from the specified C_L, the circuit oscillates at some frequency different from the nominal one.

In practice, the values of the components normally vary within the specified tolerance ranges. In the production process of oscillator circuits with the requirements of frequency tolerances lower than the tolerances of the crystal units at 25°C, an adequate reserve must be provided in the values of capacitances to meet in a simple way the condition for the oscillation at the nominal frequency. In our case, the initial value of C_2 is designed below the value computed from the above expressions. The final adjustment is accomplished by increasing the value of C_2.

The DFT switches contribute to the changes of the parameters and hence affect the operation of the oscillator. In the following we study the operation of the oscillator with inserted DFT switches in order to investigate whether the normal circuit operation can be restored.

Experiments have been performed on a 4 MHz and a 16.384 MHz oscillator implemented on a FR4

laminate (which is a common substrate for printed circuit boards) with SMD components. In both cases, transistor BFS17 and varicap diode BB619 were used. Inserted CMOS switches were of the type HEF 4066 B. At this stage, temperature compensation part has not been included.

Temperature stability (in the range of 0–50°C) of the employed 4 MHz crystal is ±20 ppm, and that of 16.384 MHz ±3 ppm, respectively. Measurements of the circuit operation have been performed at T_{amb} of 25°C ± 2 degrees, where frequency tolerance is better than ±10 ppm (for 4 MHz crystal unit), and ±5 ppm (for 16.384 MHz crystal unit), respectively.

By introducing switches S_1 and S_2 to the 4 MHz oscillator circuit the frequency decreased for approx. 112 ppm (measured at the MOS supply voltage $V_{DD} = 5$ V), and for approx. 106 ppm (at $V_{DD} = 15$ V). If only switches S_3 and S_4 were inserted, the frequency decreased for about 20 ppm (at $V_{DD} = 5$ V), and 9 ppm (at $V_{DD} = 15$ V). Finally, if all four switches were inserted the frequency changed for −137 ppm (at $V_{DD} = 5$ V), and for −113 ppm (at $V_{DD} = 15$ V), hence the effect of switches seems to be cumulative.

Further experiments have been done in the case of 16.384 MHz oscillator. At $V_{DD} = 5$ V the circuit did not oscillate, due to the impact of the inserted switches at this frequency. By increasing V_{DD}, the circuit oscillated stable at V_{DD} above 9 V, where the resistance of the switch R_{ON} falls to about 90 ohms. At $V_{DD} = 15$ V ($R_{ON} = 60$ ohms) the circuit oscillated within −100 ppm which falls within the range of the measurements of the 4 MHz oscillator.

Table 1 presents the measured frequency of the 16.384 MHz oscillator as a function of V[DD] of the inserted DFT switches. The frequency of the circuit before any DFT switches were inserted was 16.383 993 MHz.

Table 1. Measured frequency of the oscillator circuit: 16.38 MHz + f_i, $i = 0, \ldots, 3$.

V_{DD} [V]	f_0 [Hz]	f_1 [Hz]	f_2 [Hz]	f_3 [Hz]	$\triangle F$ [ppm]
10	3993	2777	3820	2329	−101
15	3993	2837	3844	2386	−98
20	3993	2903	3862	2423	−96

These terms are used in the table above:
V_{DD}: MOS supply voltage.
f_0: Frequency of oscillator without switches.
f_1: Frequency of oscillator with S_1, S_2.
f_2: Frequency of oscillator with S_3, S_4.
f_3: Frequency of oscillator with S_1, S_2, S_3, S_4.
$\triangle F$: Frequency change when all the switches are employed.

Experiments have shown that the circuit with inserted DFT switches oscillates. The change of the frequency of oscillation must be considered early in the design of the circuit. In our particular case the oscillator circuit has been first adjusted to oscillate at its nominal frequency and then the DFT switches were inserted. The frequency change has been compensated for by decreasing the value of C_2.

Precautions must be taken to minimize the effects of the DFT switches in the feedback path which results in a change of the gain and in a phase shift. The capacitive character of a switch becomes more important at lower values of C_L and higher pulling sensitivity of the crystal unit. Some designs of oscillator circuits may also be sensitive to the switch leakage current. Further work on this issue can be directed considering [13–15]. Besides, at higher frequencies, a decrease in the OFF isolation may also become the limiting factor on the performance [15]. In critical applications, frequency stability can be achieved by employing more sophisticated switches like the 1H5140 (or AD7510) series [13]. JFET DG181 is also under consideration.

The changes in the ambient temperature affect the frequency of a crystal oscillator. Among the circuit elements, the crystal is most sensitive to the changes in temperature, however other components can also be affected. Some measurements of oscillation frequency at various temperatures have been performed. Figure 5 depicts the frequency/temperature characteristics for the 4 MHz oscillator without DFT switches, and with inserted DFT switches in the temperature range 0–50°C. Notice that the oscillation frequency in the case with DFT switches is about 450 Hz lower, yet the shapes of the curves in both cases closely resemble. (Note that the left and the right hand scales are shifted

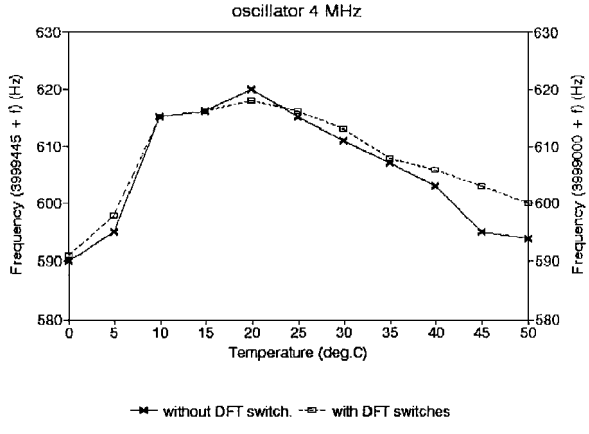

Fig. 5. 4 MHz oscillator: frequency/temperature characteristics.

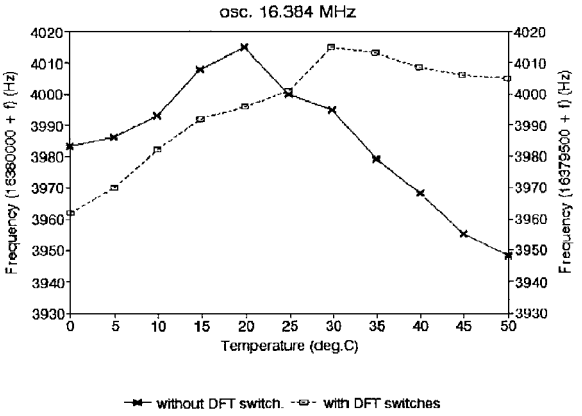

Fig. 6. 16.384 MHz oscillator: frequency/temperature characteristics.

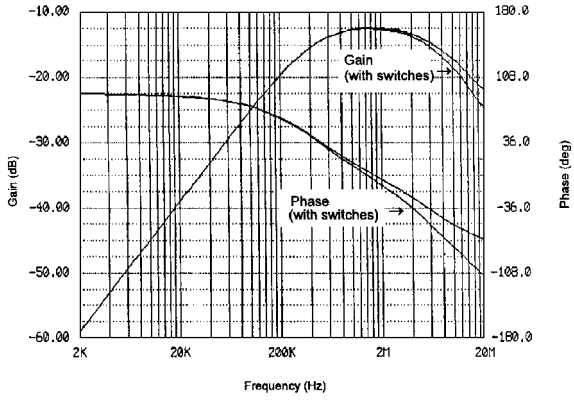

Fig. 7. Simulated feedback path characteristics (test mode 2, case 2).

against each other by 445 Hz.) By varying the value of C_2 the curve corresponding to DFT switches can get close to the original (without DFT switches). From this point, the temperature compensation can be realized in the same way as without DFT switches.

The same measurements have been repeated with the 16.384 MHz oscillator. The results are shown in Fig. 6. (The left and the right hand scales are shifted against each other by 500 Hz.) Again, the change of frequency can be compensated for by varying C_2. The impact of switches at higher temperatures affects the shape of the curve more than in the 4 MHz case. However, the temperature compensation from this point is feasible and can be done similar to the case without DFT switches.

4. Localization of Parametric Faults in Passive Circuit Components

By applying test modes 1 and 2, localization of parametric faults of resistors is straightforward.

Feedback path analysis is used in localization of parametric faults of capacitors. Here, the impact of the DFT switches on the gain and phase characteristics must be considered. Simulation results (where the switches were modeled as pure resistances) are shown in Fig. 7.

The impact of switches becomes apparent at frequencies above 2 MHz. Measurements of the prototype circuit fit closely the simulations (maximum gain difference <1 dB at gain of -60 dB). At frequencies up to 10 MHz, max. gain difference is about 1.5 dB at gain of -20 dB. Phase difference is negligible up to 500 kHz. At higher frequencies, the difference becomes apparent (for example, 7 deg. at 1 MHz).

Simulations indicate that by taking precautions in reducing parasitic capacitances and proper load adjustments the difference is supposed to lie within 0.5 dB at gain of -20 dB.

Some further steps have been taken toward a fault dictionary approach on the basis of the simulated parametric faults of capacitors. In the following we present the simulation results for the cases of faulty capacitor C_3 and faulty capacitor C_1.

Faulty C_3. Figure 8 shows gain and phase characteristics in test mode 2 (case 2) for the simulated values of C_3: 35 pF (nominal) and ± 30 pF (simulated parametric fault). The same situation is depicted in Fig. 9 for the simulated values of C_3 in the range of 35 pf$-$350 nF.

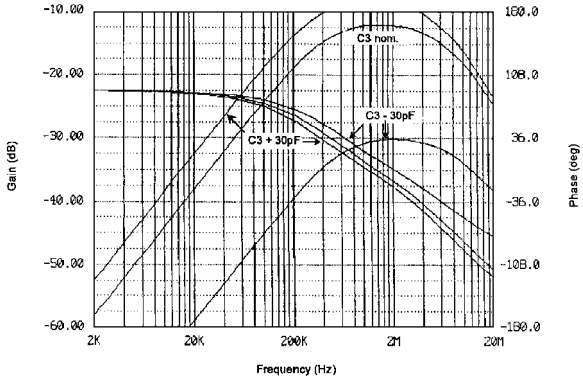

Fig. 8. Test mode 2 (case 2), simulated values of C_3: 35 pF (nominal) and ± 30 pF.

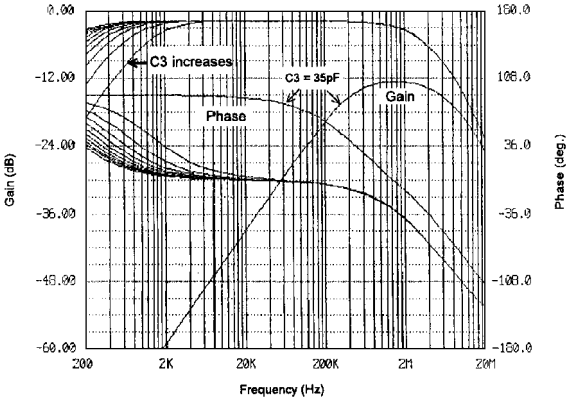

Fig. 9. Test mode 2 (case 2), simulated values of C_3 in the range from 35 pF to 350 nF.

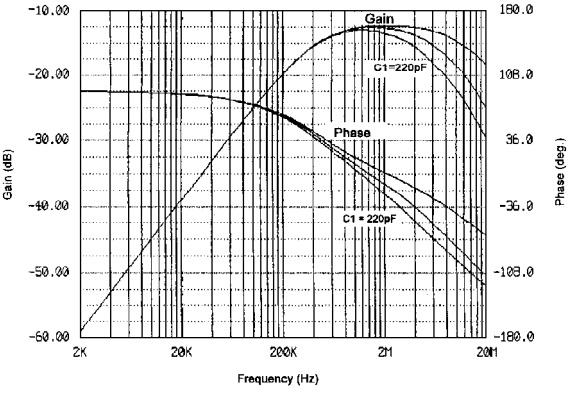

Fig. 10. Test mode 2 (case 2), simulated values of C_1: 110 pF (nominal), 1 pF and 220 pF.

Faulty C_1. Figure 10 shows gain and phase characteristics in test mode 2 (case 2) for the simulated values of C_1: 110 pF (nominal) and the simulated parametric faults: $C_1 = 1$ pF and $C_1 = 220$ pF. The change of the characteristics when C_1 was varied from 1 pF to 220 nF is shown in Fig. 11.

In practice we expect that most parametric faults lie close to the nominal values of capacitors (which is a reasonable assumption for discrete implementations). Presented simulations have been performed for wider ranges of values primarily in order to observe the trends of the changes of curves. Given fault can be associated with a specific gain-phase relationship evident from the simulated curves. Feature extraction of function behavior is supposed to provide the main information of the fault dictionary. Besides, model-based diagnosis techniques can be employed in the test mode 2 for the isolation of faulty capacitors.

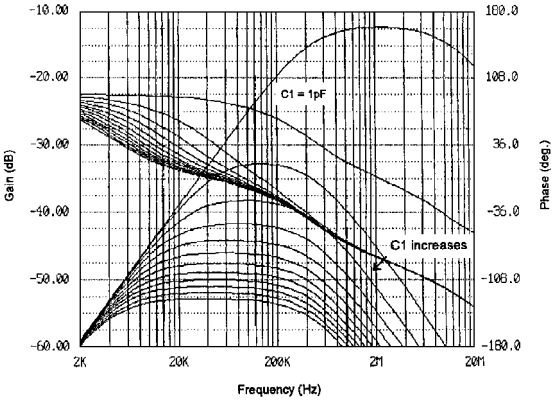

Fig. 11. Test mode 2 (case 2), simulated values of C_1 in the range from 1 pF to 220 nF.

It should be noted that the above fault isolation refers to the faults manifested at the ambient temperature $25 \pm 2^{\circ}$C. This is the reference temperature at which the crystal measurements are made according to the standards [16, 17].

Although we have focused the discussion primarily on parametric faults, presented test procedure also proved to be effective in isolation of some other assembly errors (i.e., missing components, short circuits, wrong polarity, mostly manifested as hard faults).

5. Measurements of Frequency/Temperature Characteristics of Crystal Units

For the final product, the operation of the oscillator circuit within the whole specified temperature range must be considered. The changes in temperature can affect the value of any of the components which comprise the oscillator circuit. If these component variations do not cancel each other, a change in the nominal operating frequency of the oscillator will result. The frequency determining component most severely affected by any temperature change is the quartz crystal [11].

Temperature compensation is employed in order to keep the frequency/temperature characteristics within the specified tolerances. In our case, analog temperature compensation with multiple termistor-resistor network was used to generate the required characteristics.

Temperature measurements of the assembled oscillator circuit are performed in order to obtain the necessary data for temperature compensation (i.e., for computation of the values of the elements of the circuit for temperature compensation). At the same time, the oscillator frequency/temperature characteristics are

measured. For those oscillators exhibiting abnormality such that the frequency/temperature characteristics can not be successfully compensated we proceed with fault isolation procedures.

Since we have eliminated possible faults manifested at the ambient temperature we now primarily concentrate on the verification of crystal units. Measurements of the working frequency of the oscillator circuit at the ambient temperature $25 \pm 2^{\circ}$C are performed while changing only the operating temperature of the quartz crystal in the specified temperature range. If the resulting characteristics exhibit frequency dip(s) at the same temperature(s) as the noncompensated oscillator circuit, it is very probable that the crystal unit caused the abnormal circuit operation at those temperatures.

A Peltier element is mounted on the crystal's metal case to change its temperature in the specified range (in our case: 0–50°C). At the same time, the actual temperature of the crystal is measured by a Pt 100 resistor also mounted on the crystal's case. In order to get an adequate thermal contact, thermal conductivity paste is employed. Although this measurement is not exact because it lacks the temperature stabilization of the crystal unit and the effects of the temperature of the environment cannot be completely eliminated, the method gave satisfactory results that were later confirmed by comparison with the known-good crystal units.

In the following, an example is given to illustrate the approach.

Figure 12 shows the frequency/temperature characteristics of a crystal oscillator measured in a temperature chamber. Notice that the characteristic of the oscillator already exhibits a strong temperature dependency, thus indicating that there is something wrong. The goal of the test procedure now is to identify whether this is due to a defective crystal. In the figure, characteristic of the oscillator circuit at the ambient temperature with a varying temperature of the crystal unit (Peltier) is given together with the characteristic of the crystal unit provided by the manufacturer (crystal).

A frequency dip is detected at 45–50°C. The measurement graph (Peltier) shows a frequency dip shifted from the measurements in the temperature chamber probably due to the temperature measurement imprecision presented by the graph (Peltier). The frequency dip in the frequency/temperature characteristic of the crystal unit was confirmed by simply replacing the suspected faulty quartz unit (unit 18) by a known-good crystal (unit 25). The resulting characteristic is shown in Fig. 13. More experimental results are reported in [18].

In our case study, crystal units supplied by different manufacturers have been tested on the oscillator circuit as described above. 14% of them exhibited frequency dip in the specified temperature range which could not be adequately compensated (due to the frequency stability requirements ± 1 ppm). From the specifications of the crystal units provided by the manufacturers one normally does not expect such situation. If the problem arises, crystal units exhibiting frequency dip can be easily isolated by the described approach. The problem can be solved by the additional requirements to a crystal manufacturer for factory inspection test at more

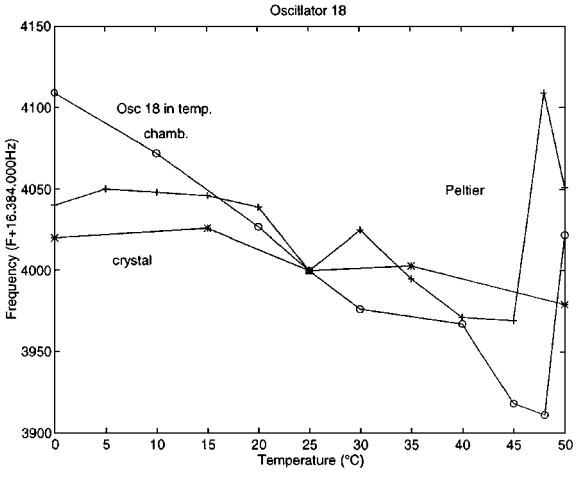

Fig. 12. Frequency/temperature characteristics of a crystal oscillator with frequency dip at 45–50°C.

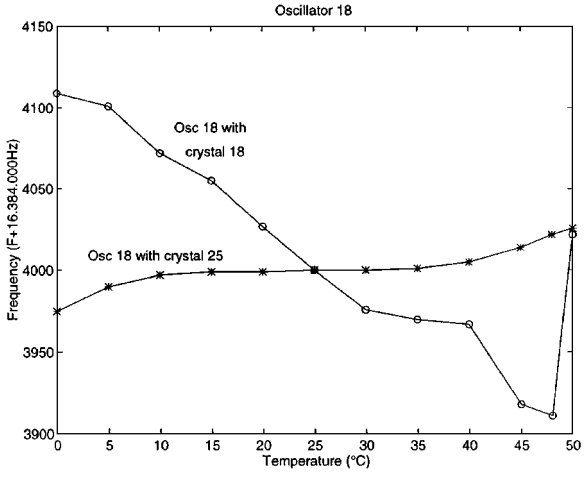

Fig. 13. Temperature compensated crystal oscillator after the replacement of the suspected faulty quartz unit.

temperature points which obviously rises the price of the crystals.

Notice that the above measurements have been performed on the oscillator circuits without DFT switches. The same procedure can be applied to the circuits with DFT switches.

6. Design-for-Test Procedure

On the basis of the presented experimental work we summarize the design-for-test procedure for crystal oscillator circuits as follows:

- Design the oscillator circuit in accordance with the required specifications and verification of its operation.
  - — Provide adequate reserve gain to function with maximum-resistance crystals plus the resistance of the DFT switches.
  - — The capacitors of the oscillator circuit are normally designed such that the impact of input and output short circuit capacitances of the transistor and stray capacitances is minimized. In the calculation of the values of the capacitors consider also the impact of the added DFT switches.
- Modify the oscillator circuit for testability.
  - — Insert the DFT switches to separate the (passive) frequency selective part from the (active) amplifier part in the way that both parts can be accessed from the existing external terminals. Otherwise, additional external test point(s) must be provided.
  - — Optionally provide for the measurements of the frequency/temperature characteristics of crystal units. Consider physical constraints in accessing crystal unit mounted on the oscillator circuit.
- Adjust the frequency of the oscillator to the nominal value by adding values of the corresponding capacitor(s).
- Generate tests, construct fault dictionary, implement model-based diagnosis procedures, implement additional measurements, etc.

7. Conclusion

Experiments have shown that the inclusion of the DFT switches in the designed crystal oscillator is feasible. As expected, the inserted DFT switches affect the frequency of oscillation. By considering their impact in the early design phase the circuit can be made to operate within the specified tolerances. Initial results confirm the advantage of the proposed approach in the prototyping phase. In our particular case, the cost of the additional DFT switches represents about 2% of the total cost of the components of the circuit. The number of switches and their positions in the circuit were chosen such that they provide for easy and effective isolation of the possible faulty components. Minimization of the number of the DFT switches remains a subject of further work on this topic.

It has been shown that for the oscillator circuit designed for testability in our case study, the selected test modes provide for easy localization of parametric faults of resistors. Parametric faults of capacitors can be isolated in different ways, for example by a fault-dictionary approach or by a model-based diagnosis.

In the design and prototyping phase, some additional measurements are often needed to distinguish possible frequency dips of the crystal unit from the other causes of improper circuit operation. An approach to a fast and non destructive verification of the operation of a crystal in a given oscillator circuit for the specified temperature range has been described. The approach gave satisfactory results that were later confirmed by a comparison with the known-good crystal units.

On the basis of the performed experimental work we have summarized a design-for-test procedure for crystal oscillator circuits. The proposed procedure is described in a general way to cover other types of crystal oscillator circuits.

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Marina Santo-Zarnik received the B.Sc. degree in electrical engineering and the M.Sc. degree in computer science from the University in Ljubljana, Slovenia, in 1982 and 1993, respectively. She is now working toward the Ph.D. degree. Since 1982 she has been working in a collaborative R&D team of HIPOT HYB, Šentjernej and Jožef Stefan Institute, Ljubljana, mainly on the development and the design of thick-hybrid circuits. In recent years, her main interests are in the area of testing and fault diagnosis of analog circuits.

Franc Novak gained the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University in Ljubljana, Slovenia, in 1975, 1977, and 1988, respectively. Since 1975 he has been with the Jožef Stefan Institute, where he is currently head of Computer Systems Department. He has also been an associate professor at the University of Ljubljana. His research interests include electronic testing and diagnosis, and fault-tolerant computing.

Srečko Maček obtained the engineering degree from the University of Ljubljana in 1971. He joined the Institute for Clinical Neurology in Ljubljana. From 1976 he is with the Cermics Department at the Jožef Stefan Institute. In 1995 he participated in the work of the Delphi group in the design of the X-ray trace detector. His research interests include hybrid technology, microelectronic materials and microwave measurements.