A 4.84 mm^2 847-955 Mb/s 397 mW Dual-Path Fully-Overlapped QC-LDPC Decoder for the WiMAX System in 0.13 μm CMOS

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Abstract

This paper presents a dual-path fully-overlapped QC-LDPC decoder for the WiMAX system. Each phase scans nonzero sub-matrices two by two in block row-wise order, and two phases are fully overlapped. It reduces memory accesses by 24.3-48.8%, and takes only 48-54 clock cycles per iteration. It is fabricated in SMIC 0.13 μm 1P8M CMOS process, which occupies 4.84 mm^2, attains 847-955 Mb/s, and consumes 397 mW with power efficiency of 42 pJ per bit per iteration.

Introduction

Due to good error-correcting performance, linear encoding complexity, and partially-parallel decoders, QC-LDPC codes [1], [2] are widely applied in the broadcast and communication systems. Improving throughput and lowering power are two trends for QC-LDPC decoders. All decoder architectures are limited to the sizes of sub-matrix ($b \times b$) and base matrix ($M \times N$). The decoder [3], advancing turbo-decoding message-passing (TDMP) algorithm, has b processors work concurrently. The decoder [4], adopting normalized min-sum algorithm, has $2 \times b$ check node updating (CNU) processors and b variable node updating (VNU) processors. The decoder [5] has $M/3$ CNU processors and $N/3$ VNU processors. However, they are short of compactness and power efficiency since both phases aren't fully overlapped. With symmetrical six-stage pipelining, block column and row interleavings, nonzero sub-matrix reordering, sum RAM partition, and read-write access bypass, a dual-path fully-overlapped QC-LDPC decoder is presented to improve throughput and lower power dissipation further in this paper.

Proposed Decoder Architecture

Fig. 1 presents our dual-path fully-overlapped QC-LDPC decoder, compatible for all 114 modes in the WiMAX system. It is built up by central controller, input/output FIFOs, ROMs, RAMs, shifters, recoverers, parity checkers, CNU processors, and VNU processors. Especially, the channel data stream is interleaved, and then written to sum RAMs for initialization. Contrarily, the hard-decision bit stream is deinterleaved before output. Each phase scans nonzero sub-matrices two by two in the block row-wise order. Sum RAMs with four independent read-write ports store not only variable node sums but also extrinsic messages as a FIFO. So it saves $20 \times 96 \times 6 = 11\ 520$ memory bits. Let (K, k) denote at the kth sub-iteration of Kth iteration, C denote message components {mag, pos, flag, sign A, sign B}, and n denote block column index.

The proposed decoder features: 1) dual-path processing; 2) fully overlapping of two phases; and 3) sharing memories by sums and extrinsic messages, so solving read-write access conflicts to sum RAMs are key issues.

To improve throughputs and help solving access conflicts, a symmetrical six-stage pipelining is proposed. Both phases are pipelined in four stages. The start and the end stages for both phases are read-write accesses to memories. Using two-port sum RAMs, the start stage of CNU phase are overlapped with the end stage of VNU phase, and vice versa. Regularly, writing operations occur three cycles later than reading operations. So the symmetrical pipelining reveals that there are no writing conflicts if reading conflicts are free.

To solve reading conflicts, three preprocessings are requisite: 1) block column interleaving; 2) block row interleaving; and 3) nonzero sub-matrix reordering. The first is to make numbers of nonzero sub-matrices in n_0 ($n\%4=0$), n_1 ($n\%4=1$), n_2 ($n\%4=2$), and n_3 ($n\%4=3$) columns as mean as possible. The second is to make sum of all correlations between two consecutive block rows including between the last and the first block rows as less as possible. The third is to make the decoder read messages from four different quadrants (n_0, n_1, n_2, and n_3) each time.

Fig. 2 demonstrates how to solve sum RAM access conflicts without FIFO for code (2304, 1/2). The upper part is the base matrix after block column and row interleavings (with original positions in the brackets). The lower part shows the rearranged updating orders of nonzero sub-matrices, sum RAM partition, and bypass and cross controlling. The updating orders for two phases are different. Here numerator is block column index n of nonzero sub-matrix, and denominator is remainder of block column index divided by four. Due to data dependency and pipelining, VNUs are delayed for six clock cycles. Two phases just read necessary messages from four different banks each time. The block column index n is used by the cross block to generate bank tag T_B ($=n\%4$) and bank address A_B ($=n>>2$). For those block columns with black down triangle, read-write accesses to sum RAMs are bypassed and the updated sums are carried from VNUs to CNUs directly. Additionally, some null operations are necessary.

Table I lists clock cycles per iteration and access decrements of sum RAMs with bypass. It only needs 54 clock cycles per iteration at most for rate 3/4 B and 48 at least for rate 1/2, 2/3 A, and 2/3 B. The read-write accesses to sum RAMs are reduced by 48.8% at most for rate 5/6 and 24.3% at least for rate 1/2. It also lists numbers of null operations required. Compared with decoders [3]-[6], the proposed decoder significantly improves throughput and utilization. Memory accesses dominate the power consumption of QC-LDPC decoders, so the large access decrements can favorably reduce the decoder's power.

Implementation Results

Fig. 3 presents the BER performance and average iteration number for code (2304, 1/2). The adopted TDMP flow results in better performance and higher convergence rate than TPMP flow. Six-bit quantization brings <0.22 dB performance loss, and satisfies performance requirement of the WiMAX system.

Fig. 4 is chip die photo of the proposed QC-LDPC decoder, fabricated in the SMIC 0.13 μm 1P8M CMOS process. There are total 80 input/output (I/O) pins with 56 signal pins and 24 power/ground (P/G) pins, and 59 memories (with numbers of each type in the brackets). Due to large successive read-write accesses, memories of the same type are placed together in

array format around the chip. The chip area is 4.84 (2.2×2.2) mm², and the core area is 3.03 (1.742×1.742) mm².

Table II summarizes the proposed and other three decoders [4]-[6] for WiMAX system. Symmetrical six-stage pipelining, block column/row interleaving, nonzero sub-matrix reordering, sum RAM partition, and read-write bypass result in the large throughput increments and high hardware utilization. The total number of memory bits is 72 552, and the count of equivalent logic gates is 470 000. Different from the other three decoders, the proposed dual-path fully-overlapped decoder only takes 48-54 clock cycles per iteration, and attains a throughput of 847-955 Mb/s at measured 214 MHz and 10 iterations. It only consumes 397 mW with much smaller power efficiency of 42 pJ per bit per iteration. The proposed decoder easily meets throughput requirements of WiMAX system at <30 MHz, and gets much better error-correcting performance at >30 iterations. Therefore, it can be flexibly tuned up to different applications.

References

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Fig. 2 Solving access conflicts without FIFO by interleaving, reordering, memory partition, and bypass and cross controlling.

Fig. 3 BER and average iteration number for code (2304, 1/2).

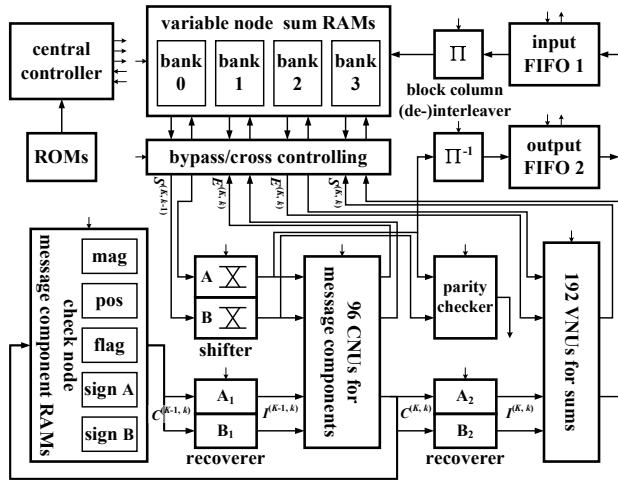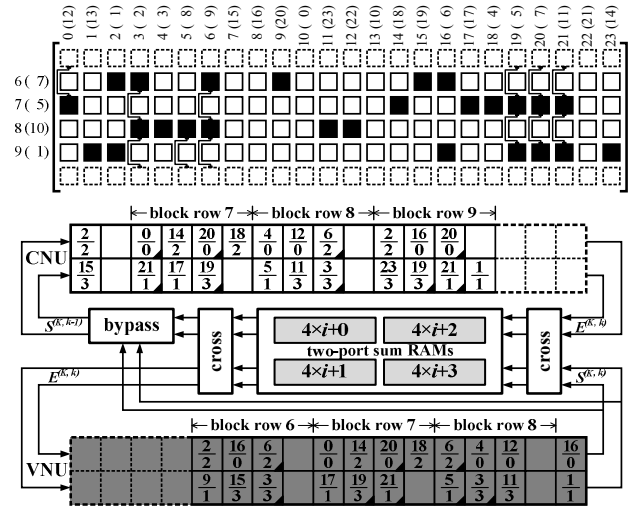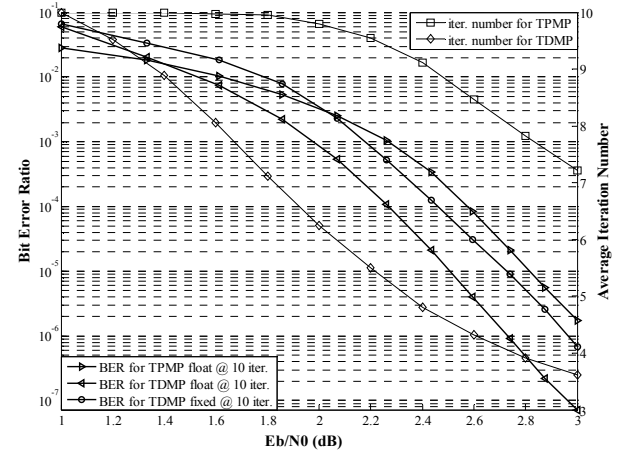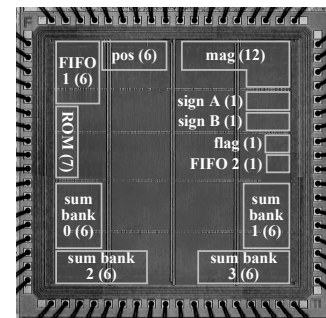Fig. 4 Chip die photo, occupying 2.2×2.2 mm².

Fig. 1 Block diagram of the proposed dual-path fully-overlapped QC-LDPC decoder for the WiMAX system.

TABLE I   CLOCK CYCLES PER ITERATION AND ACCESS DECREMENTS

	1/2	2/3 A	2/3 B	3/4 A	3/4 B	5/6
nonzero sub-matrix #	76	80	81	85	88	80
null operation #	20	16	15	11	20	24
clock cycle # per iter.	48	48	48	48	54	52
access # without bypass	304	320	324	340	352	320
access # with bypass	230	246	228	228	234	208
access decrement#	74	94	128	146	150	156
reduced by #%	24.3	29.4	39.5	42.9	42.6	48.8

TABLE II   SUMMARY OF DIFERRENT QC-LDPC DECODERS

	this work	[4]	[6]	[5]
code length	576, 672, …, 2304			
code rate	1/2, 2/3 A, 2/3 B, 3/4 A, 3/4 B, 5/6			1/2
cycle # per iteration	48-54	~160	~350	~400
quantization bits	6	6	6	8
memory bits	72 552	89 856	55 576	76 800
equivalent gates	470 000	970 000	55 000	420 000
frequency (MHz)	214	150	100	83.3
iteration number	10	20	10	2-8
throughput (Mb/s)	847-955	105	68	30-111
core/chip area (mm²)	3.03/4.84	-/6.25	3.39/-	-/8.29
power (mW)	397	264	165(sim.)	52
efficiency (pJ/bit/iter.)	42	125	243(sim.)	216
technology (μm, V)	0.13, 1.2	90, 1.0	0.18, 1.8	0.13, 1.2