# Implications of Proximity Effects for Analog Design

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### *Abstract*

This paper addresses two significant proximity effects, well proximity and STI stress, as they relate to analog circuit design. Device performance is impacted by layout features located near, but not part of the device. This adds new complexities to analog design. In either case, bias points can shift by 20-30%, causing potentially catastrophic failures in circuits. We show, for the first time, that a MOSFET placed close to a well-edge creates a graded channel.


## I. Introduction

Recent publications on the Shallow Trench Isolation (STI) stress effect [1, 2, 3, 5, 4, 6] and the well proximity effect [5, 7, 8, 9] have demonstrated the profound impact of layout variations on MOSFET performance. [2, 4] have shown that the pMOS conductivity is typically enhanced while nMOS conductivity diminished by 15-20% for MOSFETs with STI stress. Since analog designs often take advantage of efficiencies resulting from shared oxide definition (OD) regions, most designs likely incur the full range of parametric shifts due to STI stress. The well proximity has been shown to affect the threshold voltage of MOSFETs more than 1um from the well-edge. If this is not taken into account, current mirrors can be shifted out of saturation, leading to catastrophic circuit failure. Designers need to understand these new, complex barriers to compact and accurate design so that these phenomena can be anticipated.

The scope of this paper is limited to the two most profound proximity effects. There are potentially others, such as “poly-proximity” (e.g. how does the polysilicon gate of a dummy MOSFET impact the active MOSFET next to it?), and STI stress from neighboring active regions (e.g. how do the OD tiles that are used to maintain OD density for chemical mechanical polishing (CMP) impact neighboring MOSFETs?). One could even include reticle enhancement technology (RET) as a proximity effect. Methods such as optical proximity correction (OPC), as the name implies, depends on the polygon shape and neighboring features. These other phenomena may be considered small in the absolute sense, but since analog design depends on “matched” devices to attain very high precision, they may be significant.

Section II includes a description of the well-proximity effect and how matched devices, particularly current mirrors, are impacted by systematic offsets due to well proximity. Section III contains a discussion of the STI stress as it relates to multifingered MOSFETs. Various layout configurations of a ratioed current mirror are evaluated to observe the effectiveness of STI stress offset mitigation techniques. Section IV contains concluding remarks, including a discussion of CAD related issues.

## II. Well Proximity Effect

### *A. Background*

Highly scaled bulk CMOS technologies make use of high energy implants to form the deep retrograde well profiles needed for latch-up protection and suppression of lateral punch-through [10]. During the implant process, atoms can scatter laterally from the edge of the photoresist mask and become embedded in the silicon surface in the vicinity of the well edge [5, 8], as illustrated in Fig. 1. The result is a well surface concentration that changes with lateral distance from the mask edge, over the range of 1um or more. This lateral non-uniformity in well doping causes the MOSFET threshold voltages and other electrical characteristics to vary with the distance of the transitor to the well-edge. This phenomenon is commonly known as the well proximity effect (WPE).

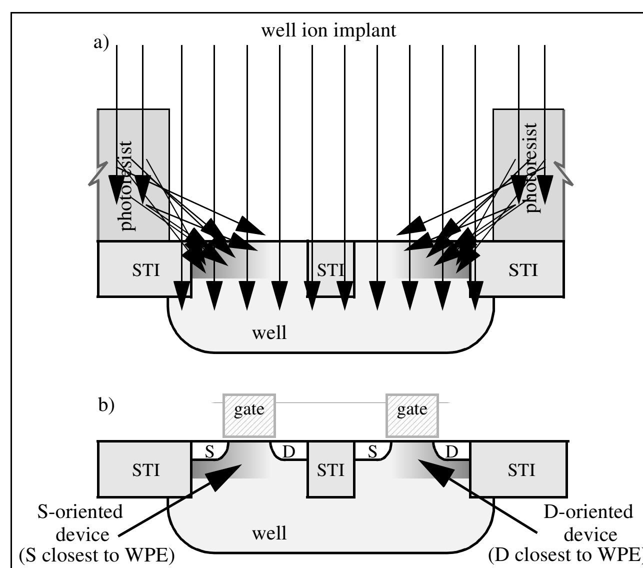


*Fig. 1: A depiction of the WPE described in* [5, 8].

### *B. Test structure*

To characterize WPE in a 0.13 um technology, arrays of thick gate (3.3V) nMOS and pMOS transistors were placed along the side of a single well edge with each device in the array located at a different well-edge spacing (Fig. 2). The other three well edges were drawn more than 25 um from the array, to ensure that only the impact of a single, isolated well edge was being evaluated.

Each array contained a single device which was located more than 25um from any well edge, far enough to guarantee it was not impacted by WPE. This device was used as a baseline, against which comparisons were made to other devices. Comparison to a baseline device isolates systematic offsets caused by well proximity from sources of global variation, in the same way that matched devices remove global variation.

The devices in Fig. 2 were routed with low resistance, symmetric source (S) and drain (D) connections, allowing the S and D assignments to be flipped. This permits S/D asymmetries introduced by WPE to be evaluated on a single device without contributions from other sources of local and global variation.

### C. Characteristics

The impact of well proximity on the threshold voltage (Vt) of the nMOS device is shown in Fig. 3. The Vt is found to increase by as much as 50mV as the device moves closer to the well edge which is consistent with previous observations [5, 8]. WPE extends roughly 3um from the well-edge. Vt is also dependent upon the S/D orientation, accounting for up to 10mV of offset.

The relative saturation current offset between transistors in the array and the baseline device are plotted in Fig. 4 as a function of Vgs. Each curve represents a different well spacing and S/D orientation. Identically sized devices can have mismatches in the drain current as large as 30% for Vgs>Vt, depending upon the proximity to a well edge. Although the Vt is consistently higher for devices with S oriented towards the well edge (S-oriented) in Fig. 3, Fig. 4 shows that the current for this device may actually be larger than the D-oriented device in the near-Vt and above-Vt regions.

### D. Implications for analog design

The impact of the WPE is considered for a current mirror application such that the well gradient is oriented in the direction of the gate length as shown in Fig. 5. This is a common layout and application, where multiple output transistors may be distributed within a common well. It is assumed that the lateral current flow in both devices in Fig. 5 are oriented in the same direction which is a standard recommended practice for matched devices. The reference transistor is far from any well-edge and has negligible well proximity induced offset.

The current mirror output is shown in Fig. 6 for various well-edge distances. This plot shows the output current of the mirror versus Vds at Vgs=1V, Vbs=0V. The dashed-line curve in Fig. 6 follows the expected behavior over Vds for a device with negligible well proximity. This curve crosses 0% where the drain bias of reference and output transistors are equal. For the remaining curves, the current offset is strongly dependent on the location of the output transistor. Even with more that 3um of distance between the well edge and the polysilicon gate, there is roughly 3-4% offset in the current.

The S/D orientation dependency shown in Fig. 3, Fig. 4 and Fig. 6 is created by the graded channel as drawn in Fig. 1b. Normalizing the S-oriented device to the D-oriented device, both nMOS (Fig. 7) and pMOS (Fig. 8) Id-Vg curves show the systematic Id offset created by graded channel. If the channel dopant is graded from the source to the drain as shown in the left transistor in Fig. 1b, the highest dopant concentration sets the threshold voltage. At the Vgs bias where the heavy doped region begins to invert, the rest of the channel has already inverted. The resultant lateral electric field enhances the

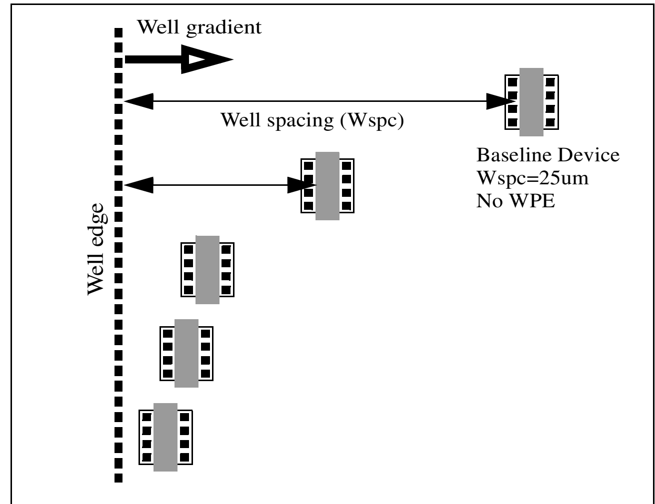


*Fig. 2: Test structure to evaluate the WPE.*

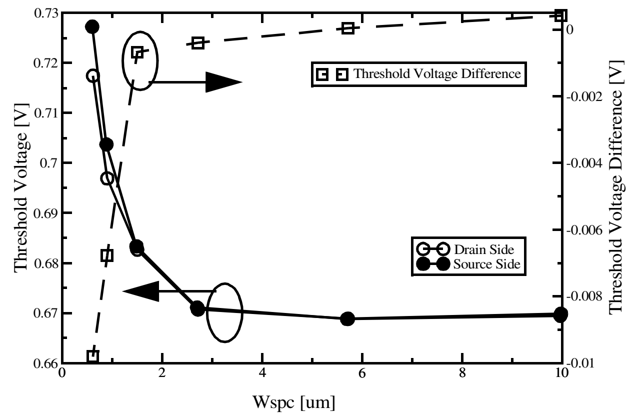


*Fig. 3: Vt versus well-edge distance for 3.3V nMOS device on a 0.13um technology.*

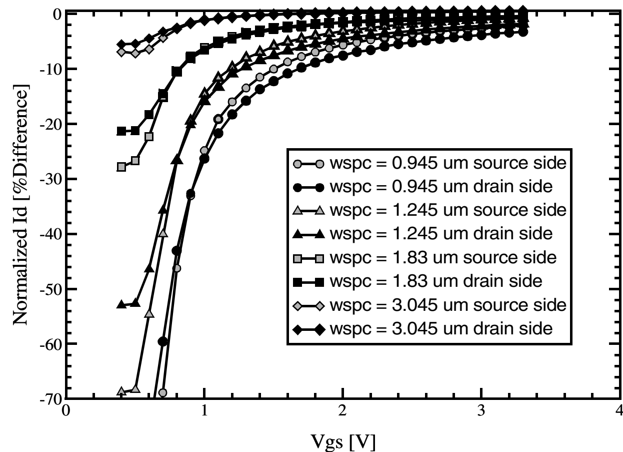


*Fig. 4: The relative difference in drain current (Id) versus gate voltage (Vg) as a function of the well-edge distance.*

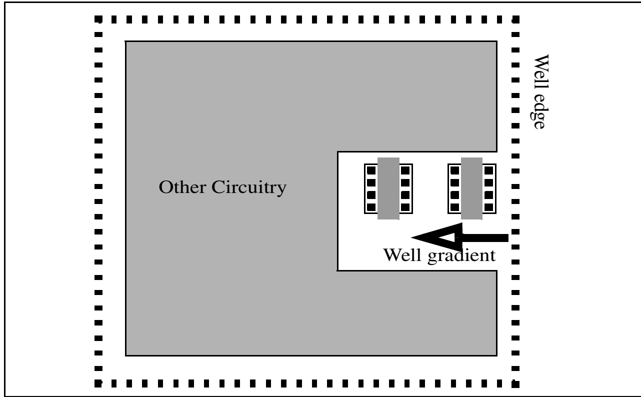


*Fig. 5: An example layout for a matched device application near a single well edge. Devices are assumed to be oriented in the same direction as per standard layout practices for matched devices to avoid S/D shadowing [5] and pocket implant asymmetry.*

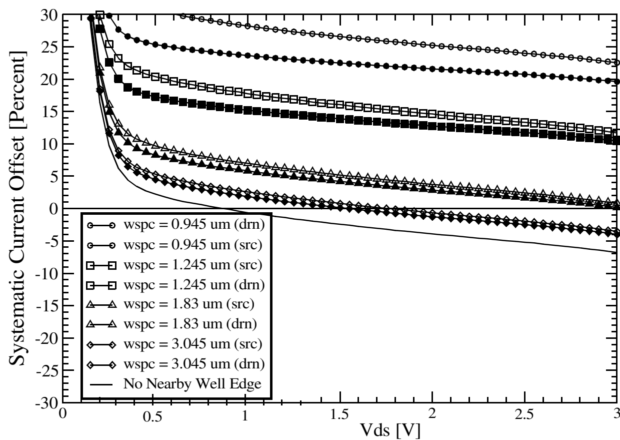


*Fig. 6: Current mirror output offset for a layout configuration as in Fig. 5 and a reference device with negligible well-proximity shift.*

channel conductivity which means that the transistor has a high transconductance (gm). A higher WPE creates a higher Vt which inhibits current flow for low Vgs, but it also creates a higher gm which enhances current flow for larger Vgs. MOSFETs with the drain oriented towards the well-edge will conduct more current at low Vgs and less current at high Vgs as compared to a device with the source oriented towards the well-edge.

Scaling of the graded channel effect is shown in Fig. 9. The device and bias conditions in Fig. 9 are identical to Fig. 8, except for the gate length which is half of the original. As the channel length decreases, the source side of the left device in Fig. 1b remains in place, while the drain side is pulled to the left. The channel still has the same peak channel dopant concentration near the source but it doesn't contain as much extent in the graded channel. This device has nearly the same Vt shift as the previous device but it has less gm enhancement which means that the cross-over point has pushed to a higher Vgs in Fig. 9. If extrapolated to smaller devices, such as thin-gate logic transistors, the crossover may not be apparent. Digital designs, which almost always use minimum length, will likely only see an effective Vt increase but not the gm enhancement. Analog designers, on the other hand, rarely use minimum gate lengths, but prefer to use lengths ranging from 2x to 8x the minimum. Graded channel modeling is paramount to analog designs with small well-edge distances.

The plot in Fig. 10 highlights a potential disconnect in characterization. This plot is the linear region sweep (Vds=0.1V) for the device used in Fig. 8. This bias does not exhibit the gm enhancement that creates the cross-over effect in Fig. 7 and Fig. 8, since Vds is low. Realizing that many devices are characterized by evaluating the Vt and gm as measured in the linear region only, the cross-over effect and the graded channel could easily be overlooked. In Fig. 10, for Vgs>1.25V, the source/drain asymmetry appears to be <0.3% but for design application in the saturated region, the offset is several times larger.

Additional Vds biases are shown in Fig. 11, for a typical gate overdrive voltage (Vgs=1V). The plots in Fig. 7, Fig. 8, and Fig. 9 were measured at Vd=Vdmax=3.3V and the plot in Fig. 10 was measured at Vds=0.1V. The plot in Fig. 11 shows that, remarkably, the worst offset is located between these two points at a bias that is often not measured but is most important for analog design, Vd=(Vgs-Vt)=Vdsat. The offset at Vdsat is nearly 2x the values measured at Vdmax, and roughly 10x larger than the WPE characterized from typical linear bias measurements.

The plot in Fig. 12 shows the impact of the WPE-induced graded channel on the output current and conductance of a device. Qualitatively, this plot is exactly the behavior that should be observed for a graded channel device as described in [11]. Although the output conductance has degraded for the D-oriented device, the shift appears to be only ~10%, compared to S-orientation.

Given the impact of the source/drain orientation, two additional layout configurations are considered. Fig. 13 contains a simple matched pair of MOSFETs that are oriented in the same direction and placed in a common well with symmetric Wspc. For the sake of simplicity and clarity in the description, well gradients originating from top and bottom well edges are neglected and the overlap of the left-side and right-side well gradients are neglected. In the latter case, a significant overlap, would mitigate the graded channel effect but the device would incur larger Vt shift from nominal. These are important considerations in SPICE modeling and CAD implementations, since the source and drain orientation are routinely flipped in the case of a multifingered device with shared sources and drains.

Fig. 14 contains a layout that might be considered as a logical solution to the WPE. This matched pair contains devices oriented in the same direction, with the same Wspc values, and the same S/D orientation to the well.

The combined WPE for layout configurations in Fig. 13 and Fig. 14 can be summed up in the plot in Fig. 15. There are four combinations of the two source/drain orientations and the two devices (output and reference). The solid line represents the expected performance of the current mirror in the absence of WPE. In both layout cases, WPE has introduced a large and

unexpected current mismatch. Considering the WPE, the design with the greatest offset would result from the layout in Fig. 13. The outer curves in Fig. 15 for these two conditions are asymmetric because one of the devices is the reference device which implies that the gate is tied to the drain. Even if the both MOSFETs are oriented in the same direction with respect to the well-edge as shown in Fig. 14, the bias points are slightly shifted because the excess dopant scattered from the well edge slightly changes the output conductance of the devices. Fig. 15 compactly demonstrates the mismatch bounds depending on the layout choices.

The existing SPICE models for well proximity consider the contribution of a well edge to be independent of orientation. Well edges located on the source, drain and width sides are all considered to contribute with equal weight. This approach misses subtleties such as the graded channel effect which have significant implications for analog design. To include these asymmetries would add significant complexity to the amount of layout related information that must be specified in SPICE simulation and/or extracted layout.

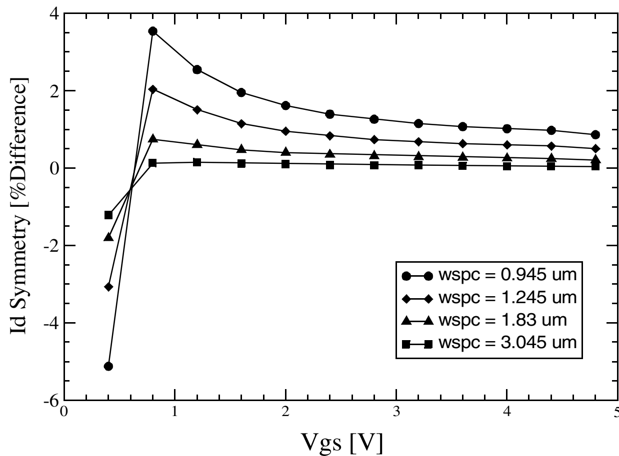


*Fig. 7: S/D Id asymmetry for a W/L=24um/1.2um 3.3V nMOS device on a 0.13um technology in the saturated region (Vds=3.3V)*

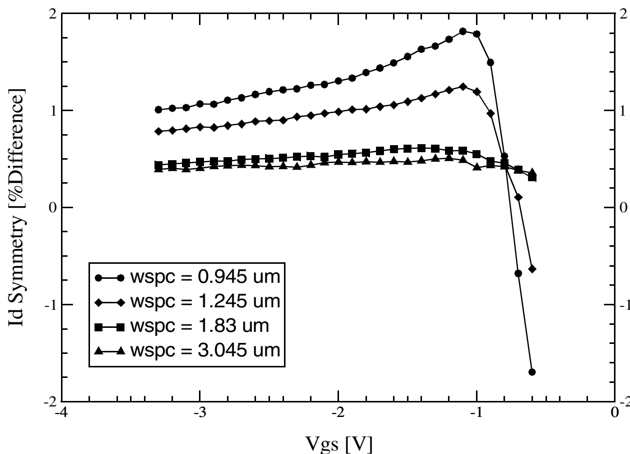


*Fig. 8: S/D Id asymmetry for a W/L=24um/1.2um 3.3V pMOS device on a 0.13um technology in the saturated region (Vds=3.3V). The apparent smoothness difference between Fig. 7 and Fig. 8 is an artifact of the voltage step size.*

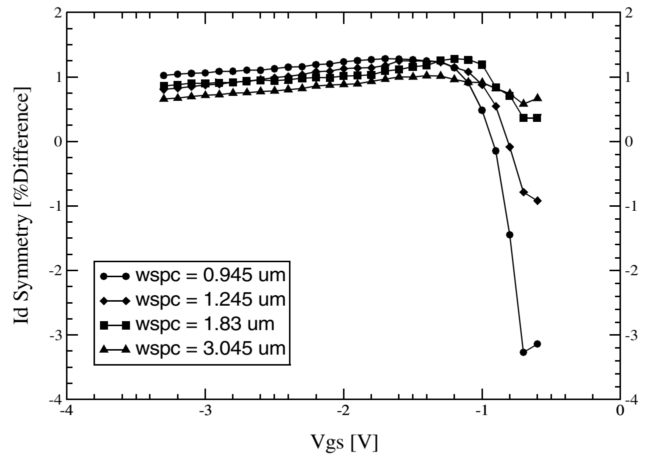


*Fig. 9: S/D Id asymmetry for a W/L=24um/0.6um 3.3V pMOS device on a 0.13um technology in the saturated region (Vds=3.3V)*

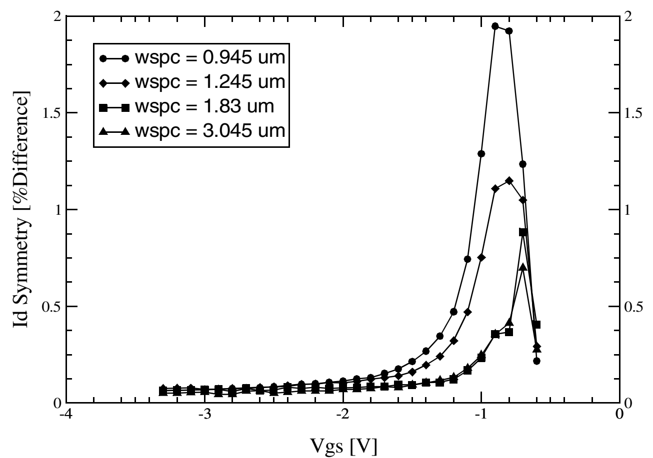


*Fig. 10: S/D Id asymmetry for a W/L=24um/1.2um 3.3V pMOS device on a 0.13um technology in the linear region (Vds=0.1V) and Vbs=0V. The crossover effect in Fig. 7 and Fig. 8 is not visible in linear region.*

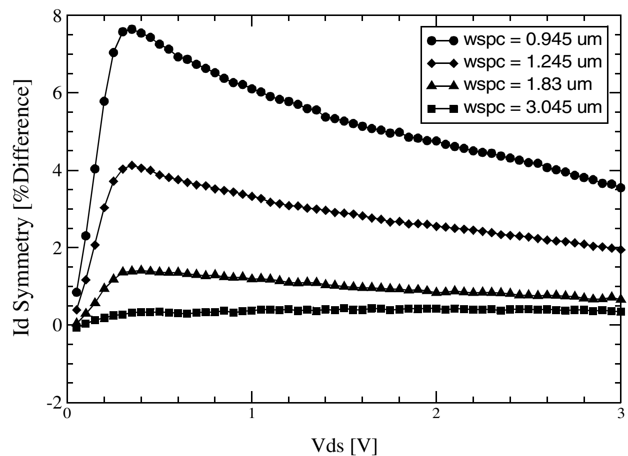


*Fig. 11: S/D asymmetry for a wide, L=1.2um 3.3V nMOS device at Vgs=1V and Vbs=0V. WPE is strongest in the region of analog design (Vd ~ Vdsat). WPE is 10x larger than the linear region measurement which is typically used for first order characterization.*

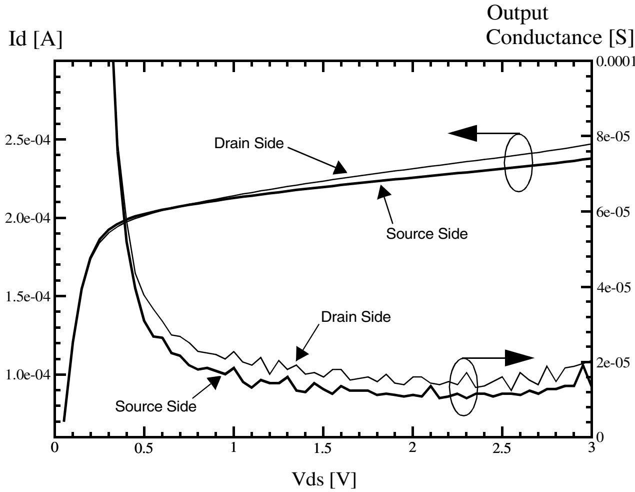


*Fig. 12: Output current and output conductance of a wide, L=0.6um 3.3V nMOS device at Vgs=1V and Vbs=0V.*

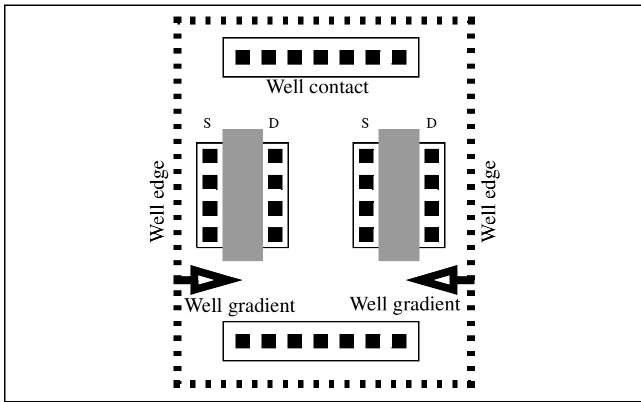


*Fig. 13: An example layout that exacerbates the source/drain orientation asymmetry due to the well proximity gradient. This layout uses a constant device orientation which is consistent with known best practices for analog layout but it is still susceptible to the well dopant gradient. See Fig. 1b for cross-section view.*

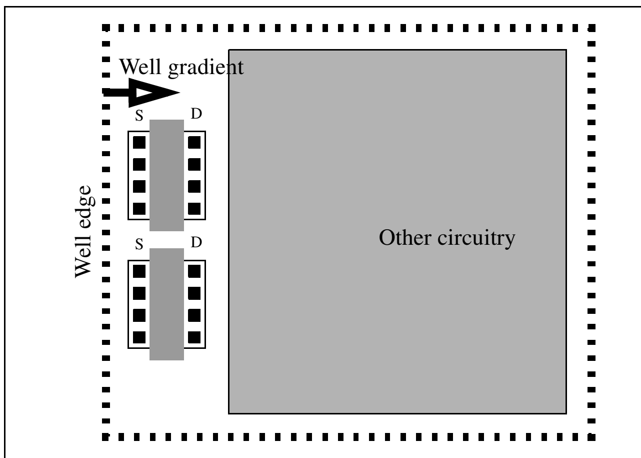


*Fig. 14: A layout configuration that may be considered in light of the WPE. Although the devices match better than the layouts in Fig. 5 and Fig. 13, the nominal performance will shift from the expected design unless the WPE is taken into account.*

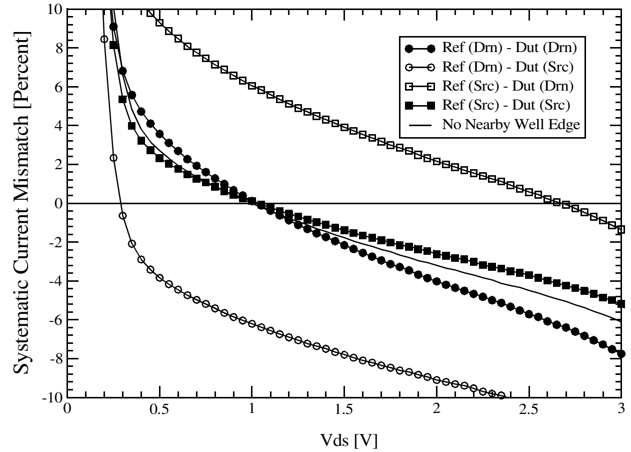


*Fig. 15: Current mirror output current, normalized to the reference current for a W/L=24um/1.2um 3.3V nMOS device on a 0.13um technology. Curves given for various orientations of the S and D with respect the well-edge.*

# III. STI Stress

## *A. Characteristics*

For sub-0.25um CMOS technologies, the most prevalent isolation scheme is shallow trench isolation. The STI process leaves behind a silicon island that is in a non-uniform state of bi-axial compressive stress [4, 2]. STI induced stress has been shown to have an impact on device performance [1, 2, 3, 5, 4, 6], introducing both Idsat and Vth offsets. These effects are significant and must be included when modeling the performance of a transistor. The stress state within an active opening is both non-uniform and dependent on the overall size of the active opening, meaning that MOSFET characteristics are once again a strong function of layout.

The STI stress effect is depicted in Fig. 16. It has been shown that the residual stress and corresponding shift in electrical performance can be qualitatively described by two geometric parameters, Sa and Sb [4, 2]. These represent the distance from the gate to the edge of the OD on either side of the device. MOSFET parameters such as Vth, peak gm and Idsat have been shown to vary linearly with the following function,

$$Stress = \frac{1}{S_a + \frac{L}{2}} + \frac{1}{S_b + \frac{L}{2}} \tag{1}$$

This relationship has been incorporated into existing SPICE models [12] to allow this phenomenon to be included in circuit simulations.

To characterize STI stress induced changes in MOSFET performance in a 0.13 um technology, arrays of thick gate (3.3V) nMOS and pMOS transistors with differing values of Sa = Sb were created. The arrays contained one device with a very large active opening (Sa=Sb=3.1 um) to serve as a baseline for comparison. A device with large Sa was chosen as the baseline because it is expected to be closest to a stress free device. The relative saturation current offset between the transistors in the

array and the baseline device are plotted in Fig. 17 as a function of Vgs. Each curve represents a different Sa, Sb value.

At high Vgs there is an increase in pMOS current with decreasing Sa value and a corresponding decrease in the nMOS current. This is consistent with the fact that bi-axial compressive stress enhances hole mobility and degrades electron mobility.

As the Vgs is lowered, the current offset in the nMOS devices increases signficantly, especially for the devices with the smallest Sa. This is indicative of a threshold voltage shift. Changes in Vt due to STI stress have been reported in the literature [2, 3] and are ascribed to stressed enhanced/inhibited diffusion.

Fig. 19 shows Idsat variation with $\langle Stress \rangle$ for additional pMOS geometries. This plot shows that the expected relationship between MOSFET performance and $\langle Stress \rangle$ holds over a range of geometries. This indicates that the STI model included in SPICE models, such as BSIM, should fit the data reasonably well and provide a reasonable prediction of the impact of STI stress on circuit performance.

The model does not include the effects of STI stress on effective channel length due to dopant redistribution, which is a phenomenon that has been proposed in the literature to explain the width dependence of Leff for pMOS device with STI isolation [1]. Fig. 18 shows a similar subtle effect from a 0.13um technology. The gm dependency on Sa , Sb flips direction as L decreases, indicating a non-constant $\Delta L$ = (Ldrawn-Leff) that is competing with the p-type mobility enhancement due to stress. The existing model [12] would not capture this trend.

### *B. Implications for analog design*

To explore the implications of STI stress, three layout configurations, Fig. 20a,b,c, for a 1:4 current mirror ratio using a 2.5V device on a 90nm technology were simulated. These layouts demonstrate the impact of STI stress on output current (Fig. 21), mismatch standard deviation (Fig. 22), Vdsat (Fig. 23), and area (Fig. 24). The non-cascoded current mirror is biased with 10uA of reference current and the reference device geometry was selected to be W/L=3.2um/0.56um to attain a Vdsat of approximately 145mV. The total width of the device was divided into 2 fingers, 4 fingers and 8 fingers in order to distribute the devices across the stress curve in Fig. 16. Each of these combinations was simulated with no dummy devices, 1 dummy device and 2 dummy devices, placed as shown in Fig. 20, to buffer the maximum STI stress near the OD-edge.

These plots show that there is substantial benefit to including dummy devices. A single dummy device appears to be very effective, and the inclusion of a additional dummy devices (i.e. place two fingers in place of the single dummy finger shown in Fig. 20) offers marginal differential return. Dummy devices can be expensive is terms of area, particularly for the block layout in Fig. 20c. Without dummy device buffers, the non-merged layout in Fig. 20b can shift the ratio to less that 1:3. Depending on the layout, Vdsat can shift over 20mV, perhaps overshooting planned design margin, and shifting the output device into the linear region.

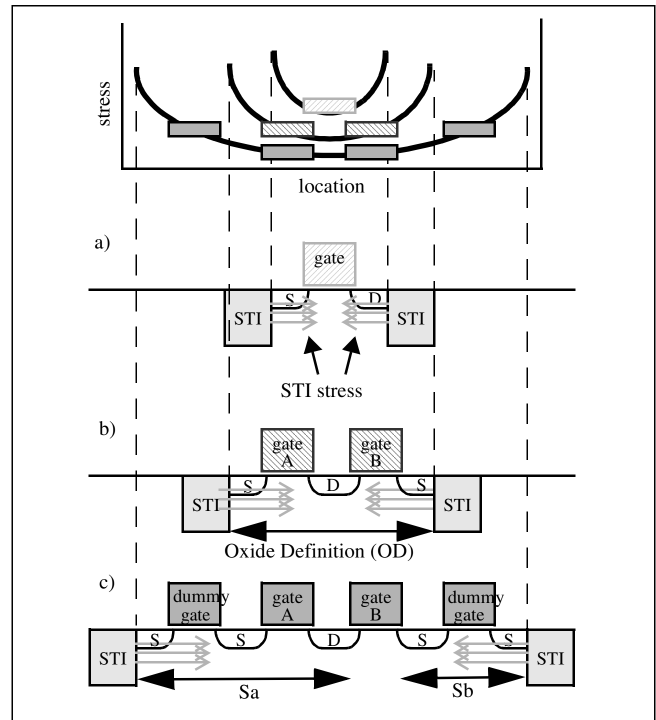


*Fig. 16: A depiction of the STI stress effect. The channel stress observed, and the resultant shift in electrical performance for a particular MOSFET is the combined effect of the size of the oxide definition (OD) region, the location of the MOSFET with the OD and the size of the MOSFET. The STI stress for a gate B in c) is characterized by the distances (Sa and Sb) of the gate edge to the OD edge. The shading of the gates in a), b), and c) coincide with the placement of the devices on the plot at the top on this Fig.*

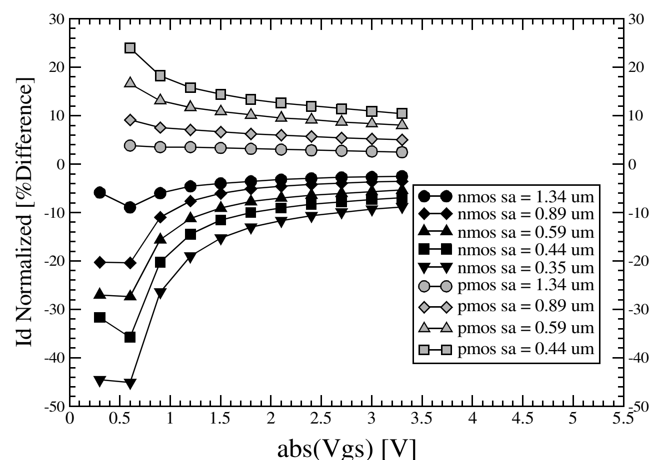


*Fig. 17: The impact of STI stress on normalized drain current for W/L=24um/0.6um 3.3V nMOS and pMOS devices in a 0.13um technology. Sa=Sb in all curves.*

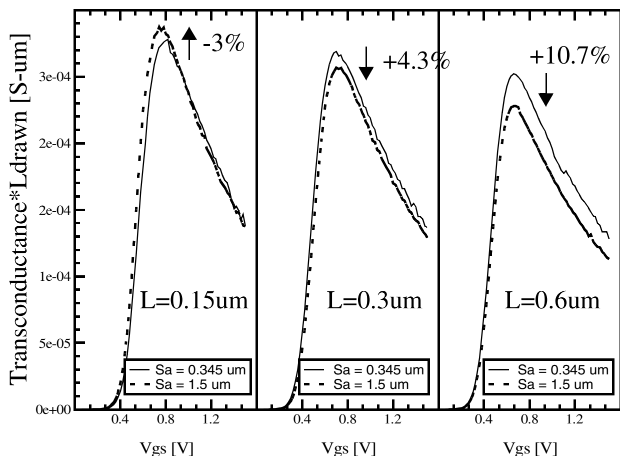


*Fig. 18: gm versus Vgs for a wide pMOS device, L=0.15um, 0.3um, 0.6um and two values of Sa,Sb. Sa=Sb in all cases.*

The biggest difficulty in handling STI stress occurs in the CAD flow for analog designs. Multifinger layouts are common practice to reduce parasitic junction capacitances, save area, and improve the effectiveness of cross-coupling (common centroid) schemes. A single transistor that is divided into multiple fingers, such as the ones in Fig. 20b,c, can be parameterized as a single instance MOSFET with lumped functional dependencies on the number of fingers and the number of dummy devices. A potential problem occurs if the parametric shift due to stress is large enough, then the bias point for each device is significantly different and a single instance MOSFET cannot physically model the multifinger device. The bigger problem is that merged, cross coupled layouts such as the one in Fig. 20a, cannot be conveniently parameterized since the connections are arbitrary. Each finger in the array has a different amount of stress and a different bias point. The only alternative is to create a separate device instance for each finger, but that impacts the size of the SPICE netlist.

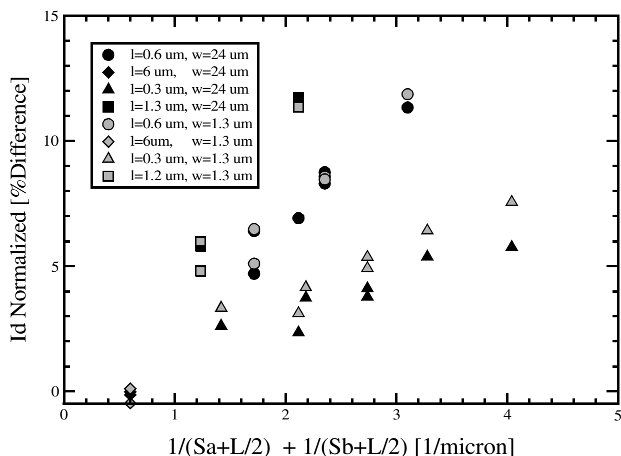


*Fig. 19: The relative shift in Idsat (Vgs=Vds=-3.3V, Vbs=0V) for a pMOS device versus STI stress for various geometries and values of Sa and Sb. Both symmetric and asymmetric values of Sa and Sb are included.*

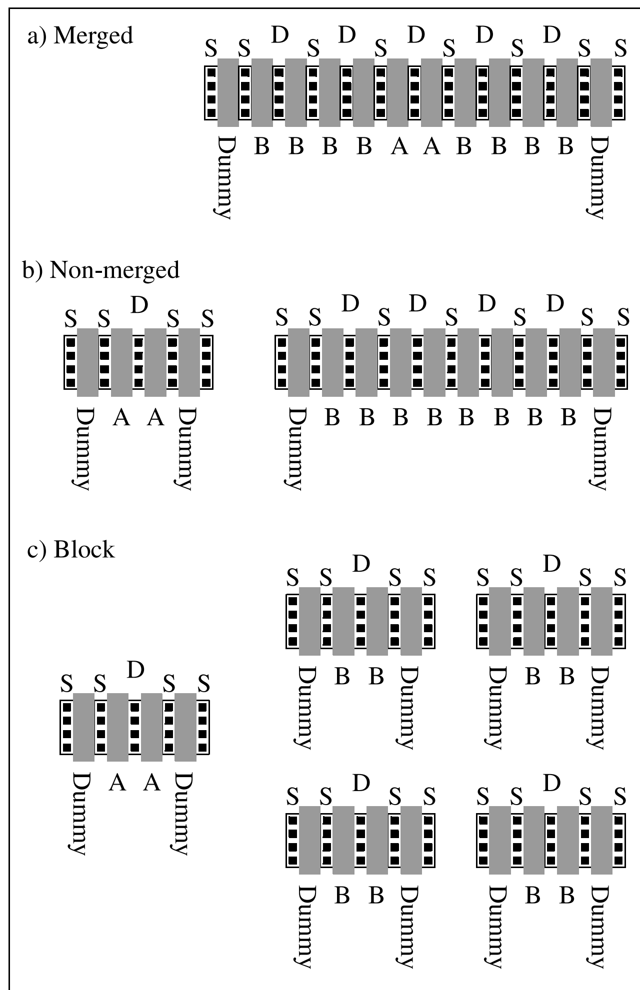


*Fig. 20: Three different matched configurations of a 1:4 (device A : device B) current mirror ratio. In the case of 2 dummy devices, 2 extra dummy gates are substituted in place where only 1 dummy is shown.*

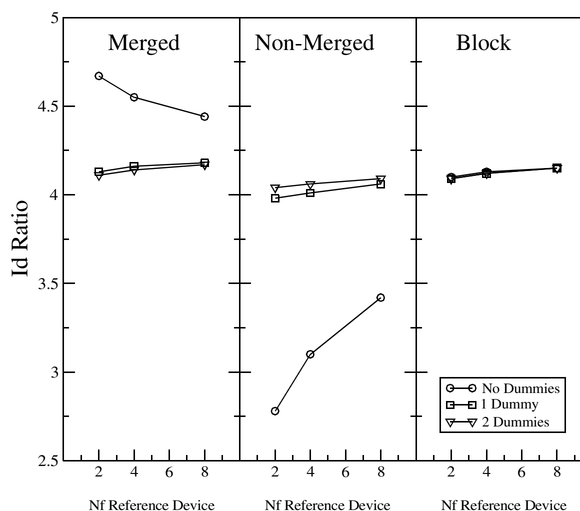


*Fig. 21: Dependence of current mirror ratio on the layout schemes in Fig. 20*

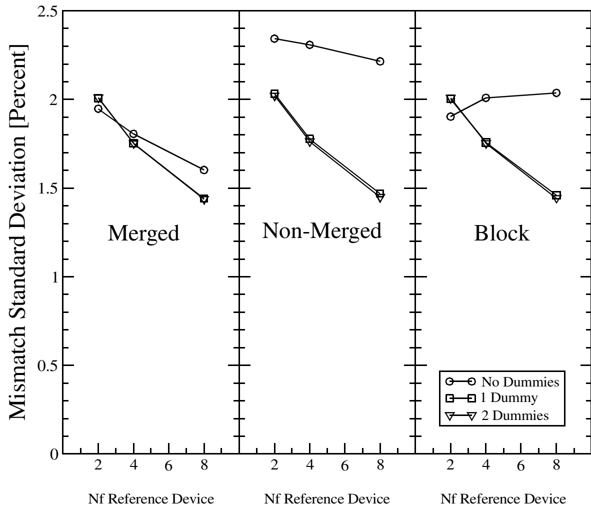


*Fig. 22: Dependence of mismatch on the layout schemes in Fig. 20*

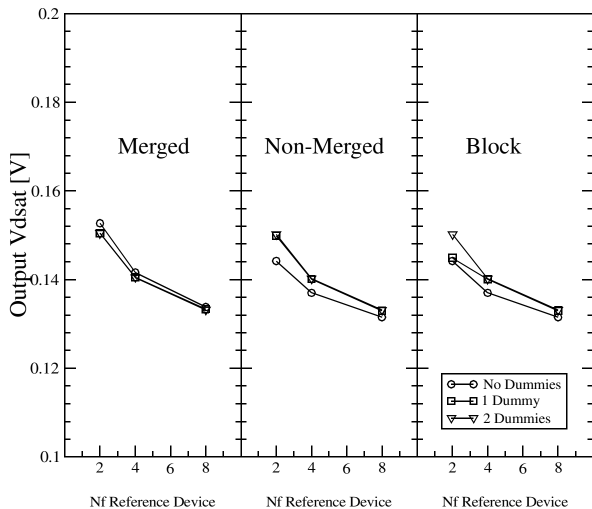


*Fig. 23: Dependence of Vdsat on the layout schemes in Fig. 20*

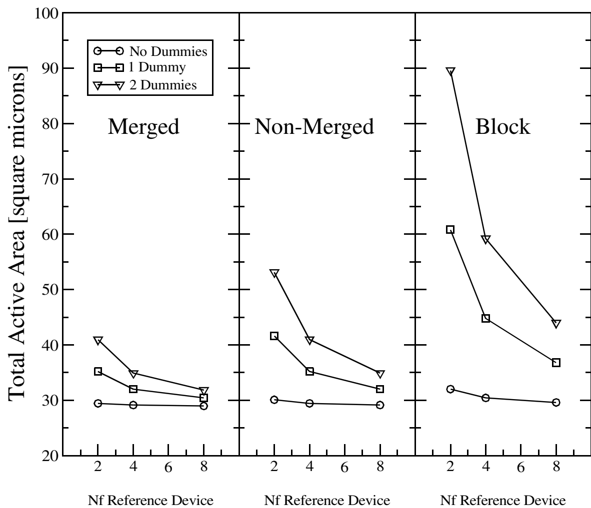


*Fig. 24: Dependence of OD area on the layout schemes in Fig. 20.*

## IV. Conclusions

This paper has demonstrated the significant impact of well proximity and STI stress on analog design. The well proximity can create a graded channel MOSFET which leads to S/D asymmetry.

An easy way around the WPE is to uniformly increase the active to well spacing. Likewise, the STI induce offset can be controlled by creating exact identical blocks for current mirror ratios. But, these solutions consume area and analog design already lags in scaling with technology shrinks due to local variation requirements (i.e. matching) and supply voltage pressures. Cost, yield and competetive pressures push designers to deal with these effects in some capacity.

Unfortunately, the nature of the problem is not conducive to industry standard CAD flow. The proximity effects are not determined until the layout stage, but the impact needs to be considered at the earlier, schematic entry and simulation stage. Backannotation of the layout attributes onto the schematic can assure consistency between layout and schematic, but this iteration sequence is tedious. Additionally, extraction of the S/D orientation from layout is problematic, since the MOSFET is symetric, and the S, D connections are arbitrary in layout.

Although some models exist for both proximity effects, in as much as the effects presented here are not included, the analog designer has absolutely no visibility into these issues within the CAD framework. No amount of simulations can otherwise account for the source and magnitude of these effects. Without any understanding of these effects, the designer is completely blind to these potential sources of catastrophic circuit failure.

## V. References


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