# The Influence of The Layout On The ESD Performance Of HV-LDMOS

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***Abstract*—The root causes of the high voltage (HV) LDMOS (Fig. 2) failed at the low voltage electrostatic-discharge (ESD) zap is found. One is caused by the bulk layout and one is caused by the intrinsic characteristic of the device. From the findings, a new structure is proposed to eliminate the root causes without sacrificing the IV characteristics and dimension of the device.**

## I. INTRODUCTION

The lateral double-diffused MOS transistor (LDMOS) [1] of the smart power technology has been commonly used in the high voltage (HV) circuits for power management, amplifier, driver and automotive ICs due to the low on resistance $R_{DSon}$ [1]. In order to ensure that the manufactured chips can pass the required ESD level, the foundries often provide the special layout rules [2] for transistors of the IO. However, this scheme will decrease the driven capability of the IO and increase the chip dimension. So, most HV-IC designs often cannot use this scheme since the IO transistor is usual a huge dimension device. The total width for IO transistor might be larger than ten thousand microns as shown in Fig. 1. Even a huge dimension IO, it sometimes cannot pass the required ESD level once it suffers the non-uniformly turned-on problem [3]. From the ORBIC picture in Fig. 1, there is only a very tiny area in such huge region appeared the hot spot due to damage. So, developing a HV-LDMOS that can meet the acceptable ESD level without scarifying the IV characteristics and dimension of the device will be a big challenge for smart power technologies.

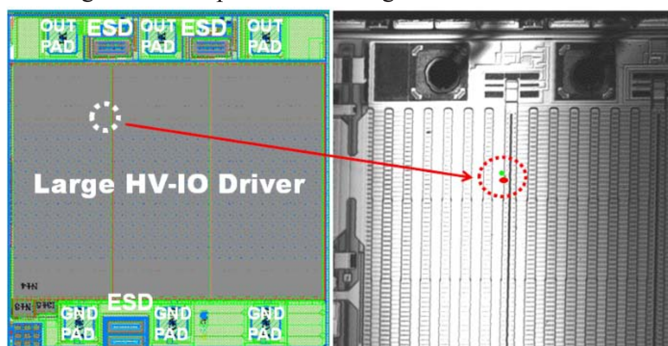


Figure 1 Layout and ORBIC picture for failure site of a large HV-IO.

## II. EXPERIENT I

The technology used to fabricate the HV-LDMOS for this work is 0.35m HV bipolar-CMOS-DMOS (BCD) process. Fig. 2 shows the cross-section of the HV-LDMOS, which includes two distinct regions. One is the channel region, which is located at the region of the P-body beneath the poly gate. In the P-body, there is a terminal (bulk) used to connect the P-body and short the source to the ground. Another one is the RESURF (reduced surface field) region [1], which is from the edge of the N+ diffusion of the drain to the edge of the channel. In this experiment, the HV-LDMOSs are all designed with multi-fingers, 30um unit finger and large total width for sustaining the high current ESD test.

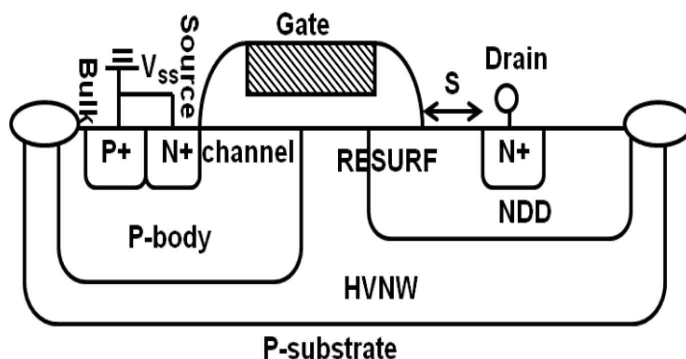


Figure 2 Cross-section of the HV-LDMOS.

### A. *Test Result for Conventional Structures*

Fig. 3 shows the layout of the conventional HV-LDMOS. It can find that the source always abuts a bulk. The N+ implants for source and drain and the P+ implant for bulk are all designed to the long strips. In this experiment, the split, N+ to poly space (S in Fig. 2) and total width (TW), is used to test the ESD susceptibility and study the failure mechanism of the device. Table I shows the layout split and ESD test result for HV-LDMOS in Fig. 3. It can find that the increase in the total width of the transistor does not increase the ESD performance of the HV-LDMOS. If the HV-NMOS is designed with the minimum S rule, it only can pass HBM 0.5KV and MM 50V.

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The increase in the S can slightly increase the device ESD performance. As the S increases to one and a half times the minimum rules, the HBM and MM can be increased to 1.0KV and 100V. As the S increases to two times the minimum rules, the HBM and MM can be increased to 2.0KV and 150V.

Fig. 4 shows the high current IV characteristics of the HV-LDMOSs in Table I under the 100nsec transmission-line-pulse (TLP) stresses. Except the HV-LDMOS with two times the minimum S rules, the leakage currents of the HV-LDMOSs are apparently increased after the first snapbacks. It is because that the HV-LDMOS is damaged by the TLP if the stress level of the TLP exceeds the trigger voltage (Vt1) of the HV-LDMOS. So, the maximum current before damage (It2) for HV-LMOS with two times the minimum S rules is apparently much higher than the It2's of other HV-LDMOSs in Table I.

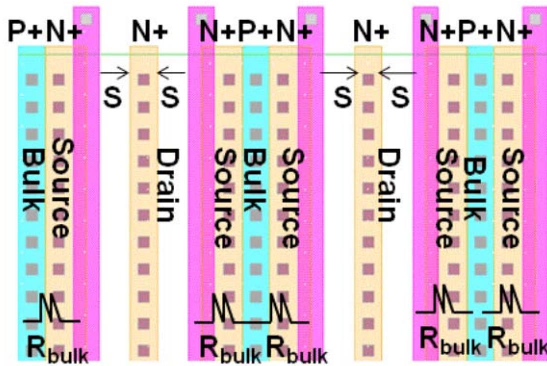


Figure 3 Conventional layout for HV-LDMOS.

TABLE I. LAYOUT SPLIT AND TEST RESULTS

| TW | S | HBM | MM | Vt1 | It2 |
|---|---|---|---|---|---|
| 120um | min. | 0.5KV | 50V | 30.5V | 0.09A |
| 240um | min. | 0.5KV | 50V | 34.5V | 0.19A |
| 360um | min. | 0.5KV | 50V | 34V | 0.28A |
| 360um | 1.5×min. | 1.0KV | 100V | 36.7V | 0.33A |
| 360um | 2×min. | 2.0KV | 150V | 43.2V | 1.07A |

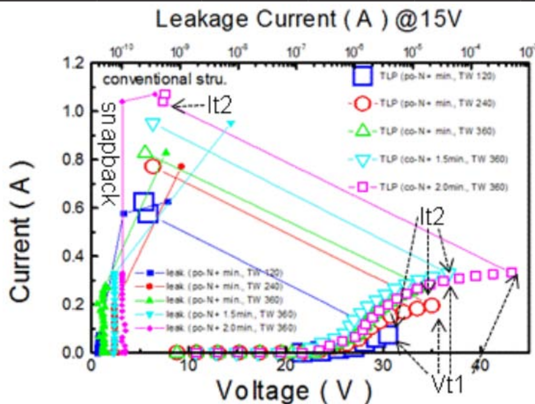


Figure 4 High current IV characteristics of the HV-LDMOSs in Table I under the 100nsec TLP stresses.

*B. Failure Mechsnism*

Fig. 5 shows the equivalent circuit for multi-fingers HV-LDMOS under +ESD/Vss zapping event. If the stress level of the TLP is higher than the Vt1 of the HV-LDMOS, the parasitic npn bipolar transistor of the HV-LDMOS will be turned on to drive the HV-LDMOS into the snapback region. It had been reported that the diode between source and P-body is needed to bias at the high-injection region as the device goes into the snapback region [4]. The criterion to sustain a stable snapback phenomenon is the potential of the P-body $V_{bulk}$ raised higher than 0.9V [4].

$$V_{bulk}=I_{bulk}\times R_{bul}\geqq 0.9V. \quad (1)$$

Since the source junction for each finger abuts a P+ diffusion, the resistance $R_{bulk}$ might be too small to satisfy above criterion for turning on the npn bipolar transistor. Even the criterion can be met, it still suffers the current crowding effect. Unlike the low-voltage NMOS fabricated on same P-substrate, the P-body for each finger of the multi-fingers HV-LDMOS is isolated from each other since they are separated by the HVNW. The parasitic npn bipolar transistor of the HV-LDMOS for each finger can be treated as an individual transistor and cannot interact with each other. As one finger of the HV-LDMOS turns on first, this finger switches into the snapback region immediately. This pulls down the voltage, resulting in the electrical fields of the other fingers too low to generate enough currents $I_{bulk}$ to turn on the other npn bipolar transistors any more. Thus, whole ESD current only can flow through this turn-on finger to cause the HV-LDMOS damaged there as shown in Fig. 6.

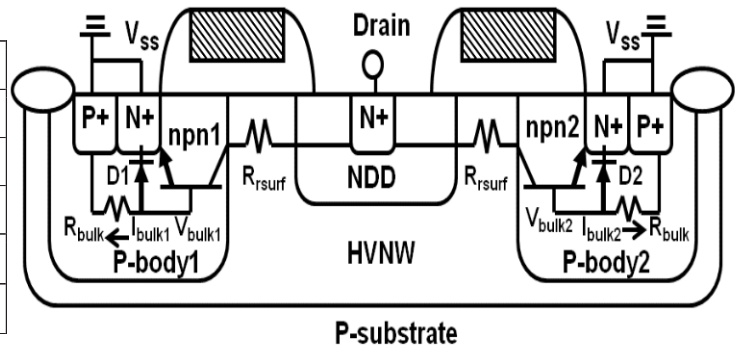


Figure 5 Equivalent circuit for multi-fingers HV-LDMOS during +ESD/Vss.

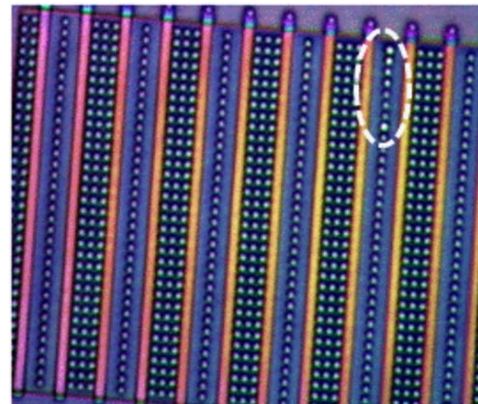

Figure 6 Damage site for conventional HV-LDMOS after HBM 1KV zap.

### C. *Discussion*

From above, the bipolar unable to turn on and current crowding effect are the root causes of the HV-LDMOS failed at the low-voltage ESD zap. If the two root causes can be eliminated, the ESD performance of the HV-LDMOS will be improved.

Although separating the bulk away the source can increase the resistance $R_{bulk}$ (Fig. 7a), the ESD performance of the device still cannot be improved if it does not have enough space between source and bulk. So, this is not a good way for ESD improvement since it is inevitable to increase the IO size. Instead of separating the bulk away the source, the new kind layout as shown in Fig. 7b, inserting some dot P+ diffusions into the source, is proposed. It not only can create the enough resistance $R_{bulk}$ but also can decrease the device dimension.

Except the current crowding effect discussed on the above, the RESURF region also can induce another kind current crowding effect. Fig. 8a shows that a turn-on finger can be depicted as a lot of npn bipolar transistors in parallel. The series resistor $R_{rsurf}$ for each npn bipolar exhibits the positive temperature coefficient of resistivity below the turn-over temperature (TOT). But, it exhibits the negative temperature coefficient of resistivity above the TOT [5]. As one region of the turn-on finger reached the TOT first, the $R_{rsurf}$ starts to decrease the resistance, resulting in more current and more power generation. Subsequently, the temperature and current increase in turn to cause the current rising higher than this region can sustain. This is why not all contacts of the turn-on finger were damaged after ESD zap as shown in Fig. 6. It had been reported that using the contact as the fuse to clamp the current can eliminate the non-uniform current distribution for fully silcided device [6]. Instead of a long strip N+ diffusion, the dot N+ diffusions are proposed to form the fuses for HV-LDMOS as shown in Fig. 9. Except acted as the fuse to clamp the current, it also can be used as the positive temperature coefficient resistor $R_{N+}$ [7] to compensate the resistance decrease caused by the $R_{rsurf}$ as shown in Fig. 8b. It is because that the TOT of the high-dosage N+ diffusion is much higher than the TOT of the low-dosage RESURF region [5].

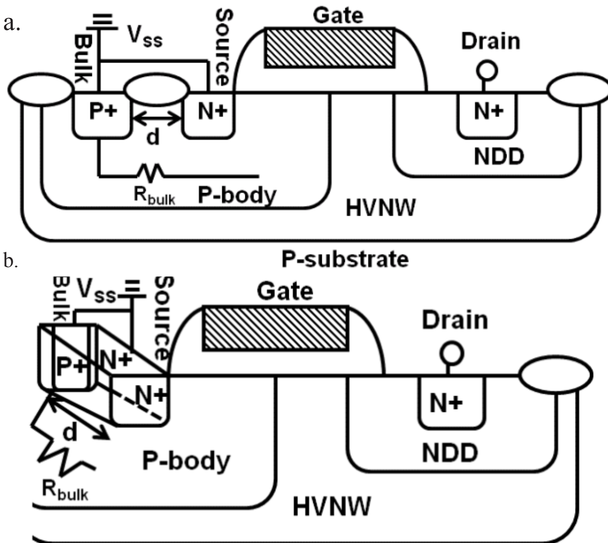


Figure 7 Two schemes to increase the resistance $R_{bulk}$.

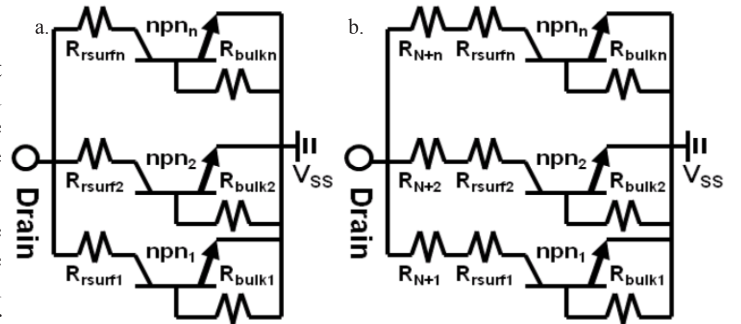


Figure 8 Schematics of HV-LDMOS for a. conventional structure in Fig. 2, b. new structure to eliminate the current crowding effect.

## III. EXPERMENT II

Fig. 9 shows the proposed structure used to eliminate the bipolar unable to turn on and current crowding effect. The new HV-LDMOS is with dot N+ on the drain and dot P+ on the source. In order not to increase the device dimension, the N+-to-po space S on the drain follows the minimum S rule of this technology.

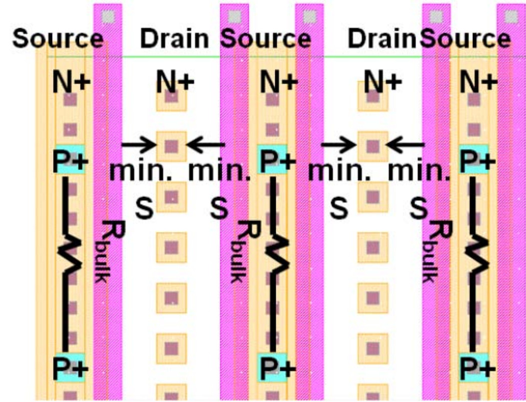


Figure 9 Layout for new HV-LDMOS.

### A. *Test Result*

Table II shows the ESD test result of the new HV-LDMOS versus the total width. Compared with the test result in Table I, the device ESD performance can be improved significantly. The new HV-LDMOSs all can pass HBM 2.5KV and MM 250V at least. Unlike conventional HV-LDMOSs with minimum S rule all failed at HBM 1KV and MM 100V, the ESD performance of the new HV-LDMOS can increase with the device total width. This implies that every finger of the new HV-LDMOS can be turned on during the ESD zap. Otherwise, the increase in the device total width cannot increase the ESD performance of the new HV-LDMOS.

Fig. 10 shows the high current IV characteristics of the new HV-LDMOSs under TLP stresses. Unlike the conventional HV-LDMOS, all new HVLDMOSs can survive after the first snapback. The It2's of the new HV-LDMOSs (>1.19A) are apparently much higher than the It2's of the conventional HV-LDMOSs (<0.28A). Moreover, it is worth noting that the Vt1 of the new HV-LDMOS (~27V) is much smaller than the Vt1 of the conventional HV-LDMOS (~34V). This implies that the new kind layout for source and bulk indeed can increase the resistance $R_{bulk}$ to make the bipolar turn on more easily. So, the HV-LDMOS would not be damaged at the snapback region any more.

TABLE II. TEST RESULTS FOR NEWSTRUCTURE HV-LDMOS

| TW | HBM | MM | Vt1 | It2 |
|---|---|---|---|---|
| 120um | 2.5KV | 250V | 27.3V | 1.19A |
| 240um | 3.5KV | 350V | 27.4V | 2.11A |
| 360um | 5.0KV | 550V | 27.8V | 2.74A |

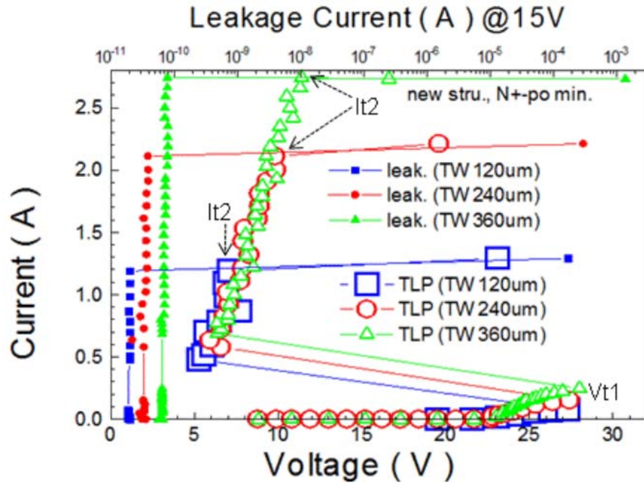


Figure 10 High current IV characteristics of new HV-LDMOSs in Fig. 8 vs. total width.

### B. *Failure Analysis and Discussion*

Fig. 11 shows the microphotograph of the new HV-LDMOS after HBM 5.5KV zap. Unlike the conventional HV-LDMOS in Fig. 6, the damages not only can be found at each finger but also can be observed at every drain contact. Furthermore, it leads to many contacts open to block the current to flow through there. A new phenomenon, the voltage shifting to the right after the It2, never being seen before can be observed in Fig. 10. This provides us the direct evidence that the dot N+ implant indeed acts as the fuse during the high current stress event. The fuse will be broken when the stress current is out of its limitation. It also proves that inserting some dot P+ implants into the source side and using the dot N+ implants on the drain can eliminate the root causes of the HV-LDMOS failed at the low voltage ESD zap. Since the whole junctions of the new HV-LDMOS during the ESD zap can be turned on simultaneously, the damages can be found anywhere in the device as shown in Fig. 11.

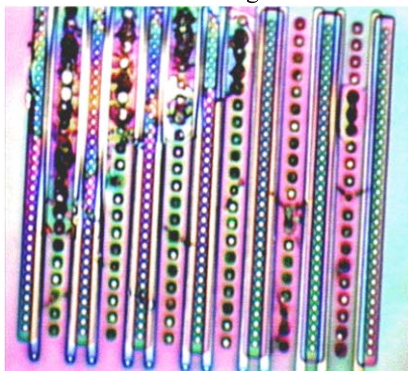

Figure 11 Damage sites for new HV-LDMOS in Fig. 9 after 5.5KV HBM zap.

### C. *DC IV Characteritics*

Fig. 12 shows the DC IV curves of the conventional and new HV-LDMOSs almost overlap each other and cannot be distinguished. This implies that the new kind layout for drain, bulk, and source does not change the IV characteristics of the HV-LDMOS. The most important is that the $R_{DSon}$ for new HV-LDMOS is decreased nearly 20% since merging the dot P+ diffusions into the source decreases the device dimension.

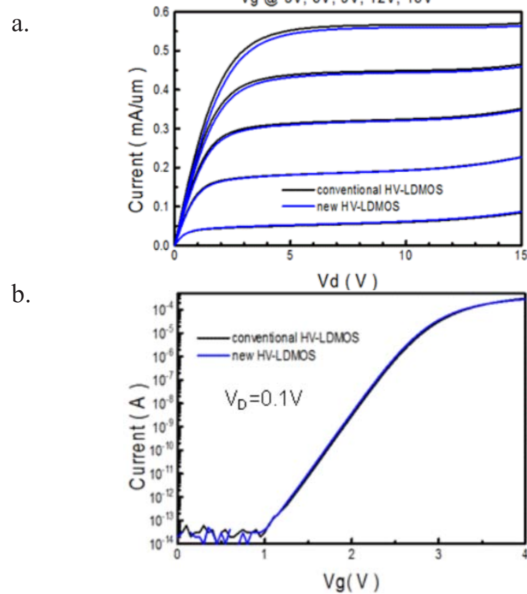


Figure 12 DC a. $I_D$ vs. $V_D$, b. $I_D$ vs. $V_G$ for HV-LDMOSs.

## CONCLUSIONS

Increasing the device dimension is not the good and unique way for ESD improvement to the HV IO transistor. Through the deeply understanding the failure mechanism of the device, the smaller and more robust ESD device can be realized from the elimination of the root causes by the layout.

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