Gate-Resistance-Limited Switching Frequencies of Power MOSFET's

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Abstract—**High-frequency switching limitation of a power MOSFET resulting from large gate resistance is studied. It is shown that a maximum gate switching frequency ($f_{G,\max}$) can be identified to minimize resistive power dissipation in the gate. Power MOSFET's with refractory silicide gates are shown to result in more than a fivefold improvement in $f_{G,\max}$ compared to conventional heavily $POCl_3$-doped polysilicon gated MOSFET's with metal gate runners.**

I. Introduction

POWER MOSFET's are the key elements of high-frequency power systems such as high-density power supplies [1]. High input impedance of an MOS gate is used to provide efficient gate control in a variety of MOS-bipolar conductivity modulated high-power devices. Gate resistance of a MOSFET has been known to result in degraded frequency response [2], [3] and to cause long-term reliability problems [4]. Conventional power MOSFET's fabricated using heavily doped polysilicon gates result in large gate interconnect resistances. Metal gate runners can be used to reduce gate resistance somewhat, but this approach leads to ineffective usage of silicon. Recently, high-temperature stable process technologies using refractory metals/silicides have been reported for fabricating high-density power MOSFET structures [5].

In this paper, high-frequency switching limitation of a power MOSFET resulting from large gate resistance is studied. It is shown that in addition to conventional high-frequency switching limitations, a new gate-resistance-limited maximum gate switching frequency ($f_{G,\max}$) can be identified. At $f_{G,\max}$ resistive power dissipated in the gate equals the power required for charging and discharging the input capacitance. For equal die sizes, power MOSFET polysilicon gates with refractory silicides result in more than a fivefold improvement in $f_{G,\max}$ compared to conventional power MOSFET's with heavily doped polysilicon gates and with metal gate runners. A fivefold improvement in gate-resistance-induced dV/dt capability and a significant reduction in total power loss is obtained for power MOSFET's with polycide gates.

II. Frequency Analysis and Results

The device structure and process technology of vertical double-diffused power MOSFET's studied in this work have been described elsewhere [5], [6]. Input capacitance C_{in} is the sum of gate-source (C_{GS}) and gate-drain (C_{GD}) capacitances where C_{GS} consists of MOS inversion layer capacitance (C_{GC}) and gate-source overlap region capacitance (C_{GO}). In this paper, the distributed RC input network of a power MOSFET gate is modeled as a series connection of R_G and C_{in}. Gate switching power loss P_{SW} is defined as equal to energy required for charging and discharging input capacitance and is given by

$$P_{SW} = \frac{fC_{\text{in}}V_{GS}^2}{1 + \omega^2 R_G^2 C_{\text{in}}^2} \tag{1}$$

where $\omega = 2\pi f$ is the angular power conversion frequency and V_{GS} is the input voltage swing. Resistive power dissipated in the gate (P_G) is separately given by

$$P_G = \frac{\omega^2 C_{\text{in}}^2 V_{GS}^2 R_G}{2(1 + \omega^2 C_{\text{in}}^2 R_G^2)} \tag{2}$$

under sinusoidal switching conditions. Conduction power loss P_C is equal to

$$P_C = I_r^2 R_{\text{on}} \tag{3}$$

where I_r is the rms output current and R_{on} is the static on-state resistance. For a given device technology, a specific on-state resistance $R_{sp}(= R_{\text{on}}A)$ and a specific input capacitance $C_{sp}(= C_{\text{in}}/A)$ can be defined independent of die area A. It has been shown that the product of R_{sp} and $C_{sp}(= k_{DEV})$ can be used as a figure of merit for evaluating performance potential of a given device technology for application in high-frequency power conversion functions [7]. Neglecting off-state power loss and that resulting from the finite reverse recovery transient of the parasitic p-n junction drain-source diode inherent in a power DMOSFET, the total power loss in a full conversion cycle (P_T) is equal to the sum of P_{SW}, P_G, and P_C. Accurate gate resistance characterization based on calorimetric power loss measurements indicated that R_G was a weak function of die area A, device geometry, and cell structure [8].

Table I lists important measured static parameters of 30-V power MOSFET's fabricated using scaled device technologies, where I_{Dsp} is the maximum peak output current-handling capability per unit die area. Capacitances listed in Table I correspond to input capacitances with drain-source terminals shorted and therefore represent the worst-case input impedance during gate switching. For a switching power supply with a specified output voltage, an optimum die area A_m can be determined to minimize P_T. Table II lists opti-

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TABLE I
MEASURED STATIC PARAMETERS OF 30-V POWER MOSFET'S

Parameter	Unit	Polysilicon Gate	Polycide Gate
I_{Dsp}	A/cm^2	600	600
R_{sp}	$m\Omega\text{-}cm^2$	0.35	0.29
C_{sp}	pF/cm^2	38,400	36,800
k_{DEV}	$pF \times \Omega$	13.5	10.7
R_G	Ω	1.5	0.3

TABLE II
OPTIMUM PERFORMANCE OF 30-V MOSFET'S IN A 100-W, 5-V, 10-MHz POWER SUPPLY

Parameter	Unit	Polysilicon Gate	Polycide Gate
I_r	A	14.1	14.1
V_{GS}	V	10	10
P_C	W	2.15	1.6
P_{SW}	W	1.23	1.33
P_G	W	0.45	0.11
P_T	W	3.83	3.04
Die Size	mil x mil	72 x 72	76 x 76

mized power MOSFET parameters for a 100-W, 5-V, 10-MHz power supply where die size corresponds to packaged device dimensions. These results suggest that for a 5% larger die size more than a 20% lower power loss results by replacing conventional polysilicon gates with polycide gates.

In many high-frequency power switching systems it may be possible to recover P_{SW} by using a resonant switching topology. Resistive power loss in the gate, however, cannot be recovered. Power loss calculations were performed for 30-V power MOSFET's using the static parameters listed in Table I. These calculations were first performed versus switching frequency where conduction current corresponded to maximum output current-handling capability for a 100-mil die. Power MOSFET's with polysilicon gates resulted in a significantly higher power loss. Gate power loss P_G increased rapidly with frequency and eventually exceeded P_{SW}. A maximum gate switching frequency $f_{G,\max}$ was identified where $P_G = P_{SW}$. Table III lists the calculated values of $f_{G,\max}$ for the 30-V power MOSFET's studied here. For comparison, conventional switching frequencies are also listed in Table III where f_{in} corresponds to the switching frequency limited by the input gate RC time constant, f_M is the maximum frequency of operation where gate current becomes equal to output current, and f_T is the transit-time limited frequency [1]. In Table III, g_m corresponds to linear region transconductance, μ_n is the MOS inversion-layer electron mobility, C_{ox} is the gate oxide capacitance per unit gate area, L_{CH} is the MOS inversion channel length, W_{CH} is the channel width, L_D is the drift region length, and BV_{PP} is the breakdown voltage of the p-base to n-epi parallel plane junction. Switching frequency limitations imposed by f_M and f_T far exceed those caused by f_{in} and $f_{G,\max}$. Thus, the maximum switching frequency of a power MOSFET may not exceed $f_{G,\max}$, beyond which gate resistive power dissipation becomes excessively large. Fig. 1 shows f_{in} and $f_{G,\max}$ as a function of die size assuming a square die. These results suggest that more than a fivefold improvement in $f_{G,\max}$ can be achieved using polycide MOS gates.

TABLE III
MAXIMUM SWITCHING FREQUENCIES AND dV/dt CAPABILITIES OF OPTIMIZED 100-MIL × 100-MIL, 30-V POWER MOSFET'S WITH V_{GS} = 10 V, L_{CH} = 1 μm, L_D = 4 μm, V_T = 2 V, AND BV_{PP} = 35 V

Parameter	Unit	Formula	Polysilicon Gate	Polycide Gate
g_m	Ω^{-1}	$\frac{\mu_n C_{ox} W_{CH} I_{Dsp} R_{sp}}{L_{CH}}$	51	42
$f_{G,max}$	Hz	$\frac{1}{2\pi^2 C_{in} R_G}$	14×10^6	73×10^6
f_{in}	Hz	$\frac{1}{2\pi C_{in} R_G}$	44×10^6	230×10^6
f_M	Hz	$\frac{g_m}{2\pi C_{in}}$	3.4×10^9	2.9×10^9
f_T	Hz	$\frac{6.11\times10^{11}\, BV_{PP}^{7/6}}{(1+\frac{L_{CH}}{L_D})}$	7.7×10^9	7.7×10^9
$\frac{dV}{dt}$	$V.sec^{-1}$	$\frac{V_T}{R_G C_{GD}}$	7.4×10^8	3.8×10^9

A important switching limitation in power devices results from the rate of change of output voltage or the dV/dt capability. In a power MOSFET, for example, a parasitic gate turn-on may occur if the rate of change of output voltage is sufficient to produce a threshold voltage drop across gate resistance [1]. This situation results from current flow into the input circuit because of voltage fluctuations across C_{GD}. The resulting dV/dt capability is given by

$$\frac{dV}{dt} = \frac{V_T}{R_G C_{GD}}. \tag{4}$$

A fivefold improvement in dV/dt capability is obtained for power MOSFET's with polycide gates as shown in Table III.

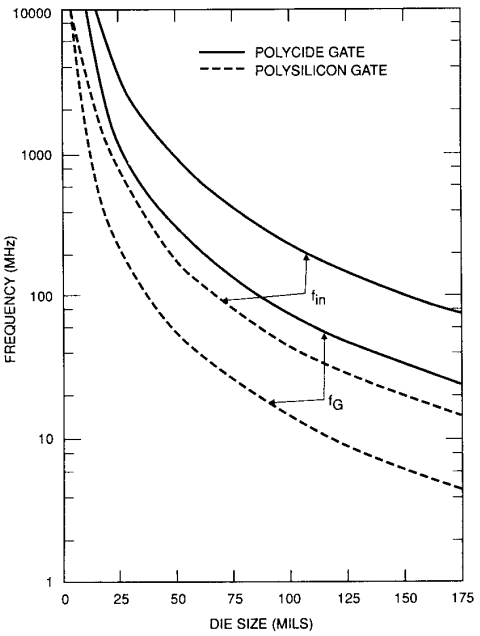

Fig. 1. Switching frequencies versus die size for 30-V power MOSFET's. The values of f_M and f_T listed in Table III are independent of die size.

III. Discussions and Conclusions

It is shown that nearly a fivefold reduction in gate resistance can be obtained by incorporating refractory metals/silicides on power MOSFET polysilicon gates. Input switching frequency limitations resulting from large gate resistances are studied. A maximum gate switching frequency $f_{G,\max}$ is identified beyond which resistive power dissipation in the gate becomes excessively large. Power MOSFET's with polycide gates are shown to result in more than fivefold improvements in $f_{G,\max}$ and output dV/dt capability.

In a number of power converters such as those employed in automotive electronics, telecommunication, power supplies, display drives, motor control, and medical electronics, power devices with die sizes in excess of 100 mils on a side are common. In addition to imposing severe frequency switching limitations, large gate resistance can lead to destructive long-term failure modes of operation. In such circuits, in addition to minimizing the gate interconnect resistance, series resistance of gate driver circuit should also be reduced. However, gate interconnect resistance takes a higher precedence here as it directly impacts unit cells that constitute the power device.

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