The Failure Mechanism of Gate Resistance Testing for Power MOSFET

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Abstract

The vertical DMOS (Double Diffused MOSFET) is widely used in power microelectronics, its switching performance is determined mainly by the gate resistance and the input capacitance. Thus a gate resistance testing technique is developed in order to determine its device functionality. In this paper we will discuss various processes induced device failures, such as the poor interconnect of the poly gate and the metal, the bonding wire, and the etch process, and their impact to the performance and reliability of the devices as well as the in-line testing method used for the performance validation.

1. Introduction

Power MOSFET is widely used now as a switching power supply device for appliance, computer, automotive and other application. Today the vertical structure DMOS in both planar and trench structures [1] have good performance with low conduction resistance RDS(on) which determines the power dissipation of themselves, and with the optimization in the process and package technology for their switching speed and ruggedness for operating in extreme electrical and thermal conditions. The switching speed depends on the parameter of gate charge and the ruggedness for electrical and thermal stress depends on the breakdown voltage of the device. In fact the switching speed, the conduction resistance and the ruggedness performance need to consider in the same time in order to estimate the tradeoffs and performance optimization from the point of process technology and package technology.

For power MOSFET now switching speed is determined mainly by the gate charge that a device needs to turn on itself [3]. So the time required to turn on and turn off depends on the charge and discharge process of the device, this is determined by the time constant RG*CG. So increasing switching speed with constant gate charge is necessary to reduce the gate resistance and input capacitance.

In order to characterize the device's switching performance, the gate resistance testing is performed. From the testing result, the devices with poor switching performance can be screened out, and from the failure analysis, the processing induced defects can also be investigated to improve the device's yield and reliability.

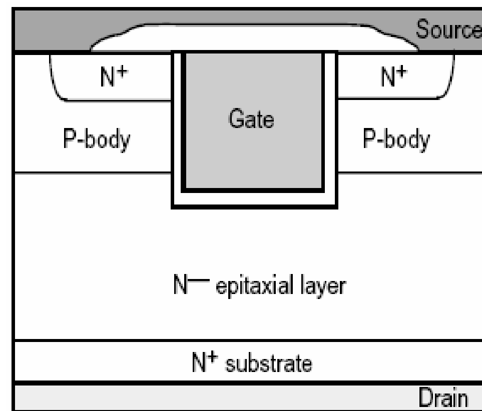

Figure 1 Trench structure VDMOS

2. Gate resistance model and its testing condition

Power MOSFET has one advantage that it is a voltage controlled device, the input resistance is very high due to the gate oxide insulation, thus the drive circuit is simple and the drive power dissipation is very low. In fact it can be considered by its parasitic impedance, the real part is the gate resistance and the imaginary part is the reactance of the gate capacitance, as in equation (1).

$$Z_g = R_g + \frac{1}{j\omega C_g} \quad (1)$$

From figure 2, the gate resistance is equivalent to the resistance of the input gate, the same to the conduction resistance RDS(on) [1], the source resistance, the channel resistance, and the accumulation resistance of the drift area all contribute to the gate resistance as in figure 1. Besides the poly gate and the interconnect resistance of the metal can also contribute the gate resistance.

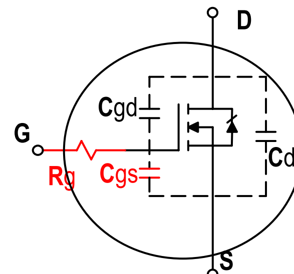

Figure 2 The gate impedance model

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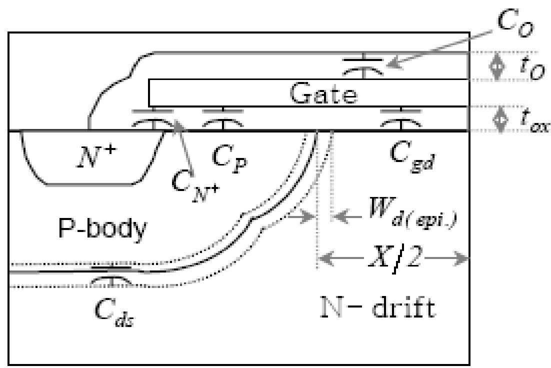

Figure 3 The gate capacitance

The gate capacitance's model can be seen from the figure 2, it includes the Cgs and Cgd, the Cgd is the miller capacitance, it is influenced by the voltage between the gate and the drain, the Cgs physical model is as below in figure 3. It has 3 parts: C_P is the capacitance between the poly gate and the p body area, C_O is the capacitance between the poly gate and the source metal, the dielectric is the BPSG layer, C_{N+} is the capacitance between the poly gate and the source area.

$$Cg = Cgs + Cgd \qquad (2)$$

$$Cgs = C_{N^+} + C_O + C_P \qquad (3)$$

When device turns on and turns off, the charge time and discharge time depend on the product of Rg*Cg, and during the switching process, the gate resistance will dissipate energy, this can also lead to power dissipation. So the gate resistance is an important figure of merit for power MOSFET.

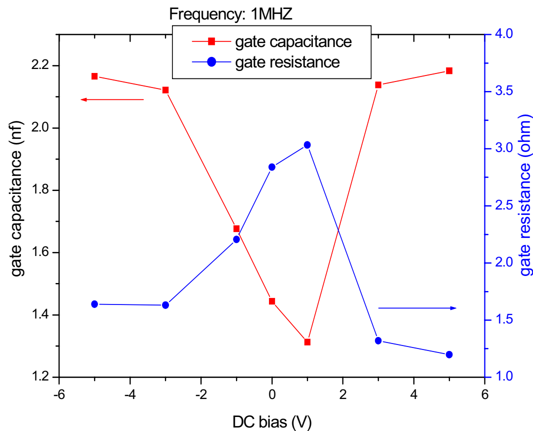

Figure 4 The gate bias's effect to Rg and Cg

During the testing, the drain is short to the source, and an AC signal is imposed between the gate and the source. The testing results can be greatly affected by the frequency and the bias voltage. A testing condition's effect is shown in figure 4 and figure 5 for a trench power MOSFET.

From the date above, enough gate bias in both negative and positive directions will reduce the gate resistance and increase the gate capacitance, because the gate bias will introduce enough carriers in the channel and the accumulation area. The frequency's modulation can affect the gate resistance when the bias is not high enough caused by the mismatch between the carrier velocity and the signal frequency [2]. For our testing experiment, the frequency is set to a fixed value at 1MHz.

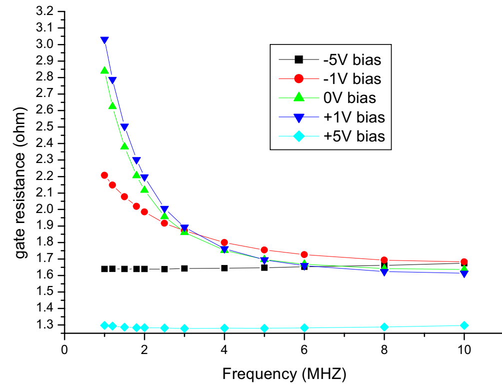

Figure 5 Frequency's effect to gate resistance

3. Failure Mechanisms

From the testing, some failures can be uncovered which are induced by the defect of processing. In order to have a good performance and reliability of the device, the failure mechanisms must be discovered.

One of the failures is due to the poor conductivity of the interconnection for the poly gate and the metal of the gate bus line. The doping level of the polysilicon gate, the gate conducting fingers, the interface of the poly gate to the metal can all be detected by the testing, for example: the low doping level of the poly gate, the poor silicidation process and the anneal process, the poor clean of the interface between the poly gate and the metal, the poor ohm contact of the interface between the metal and the poly gate will all lead to high gate resistance and longer switching time.

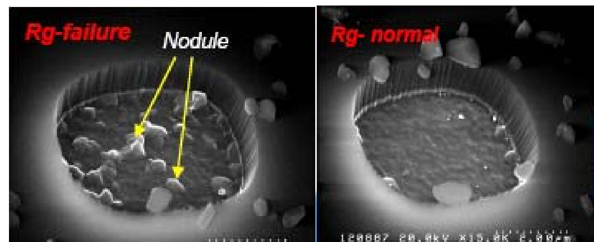

Figure 6 The SEM of the interface for fail and normal

From the failure analysis, such failure can be found as shown in figure 6, the etching and clean process is not satisfactory and there is some residue left at the interface, so the gate resistance is high and the switching time is

too long.

Another type of failures also relates to the interconnection process, which is the wire bond process during the package. Bonding wire is used to connect the die and the lead frame to realize the electrical connection of the device. The bond pad interface and the inner lead interface of the bonding wires can be lifted off due to the degradation of the interface from the oxidation or formation of intermetallic compounds at the interface [4]. Such poor contact can also lead to high gate resistance. Because the power MOSFET exhibits high current, as the Al wire is used, the intermetallic compound effect at the interface is not common, since the pad is also made of Al. But the inner lead of the lead frame interface is easy to oxidize though there is a plating layer. Most of the lead frame is the made of Cu or Fe/Ni alloy, the plating layer used is the Ni/Ag alloy. For this material system, during the bonding process must be taken care for the existence of the poor contact interface. Besides that, the bonding wire heel area stands high thermal mechanical stress during the reliability testing and the working environment, its wearing out will lead to crack at the heel, as in figure 7.

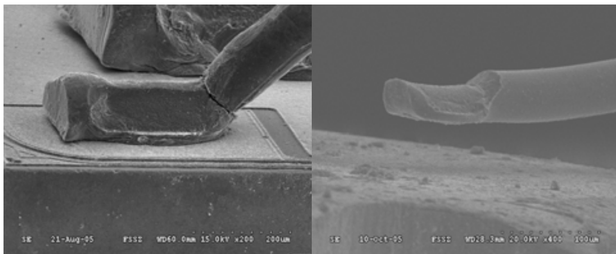

Figure 7 The SEM of the bonding wire lift off and heel crack

Other than the process defect described above which leads to high gate resistance, there are still other effects that can cause high gate resistance.

One of them is that when the device gate is leaky, the gate electrode is short to the device source; the gate resistance can be measured higher. This is due to that the gate oxide now loss the capacitive property, so the gate resistance is just a physical resistance of the return path, there is inversion layer and accumulation carriers below the gate, the channel resistance is very high. In other words, the device will dissipate more power when short, so the result is high gate resistance. Once the device gate is short to source, its gate resistance is above 50 ohm, for the normal device the gate resistance is measured below 5 ohm. So this gate capacitance's modulation effect is very important for the channel and the accumulation area below the gate oxide, it determines the amount of the carriers. Such failure result can be seen in figure 8. From the SEM, it can be found that the Al diffused into the BPSG layer and caused the device short.

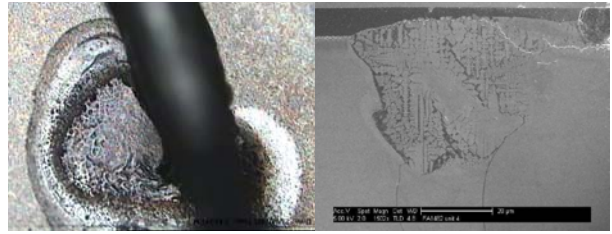

Figure 8 The burnt point of the source metal and the Al diffusion to the BPSG layer

From the testing result and failure analysis, It is found that the thicker BPSG layer can also lead to higher gate resistance. As in figure 9, the BPSG layer of the failure is over 0.4um, but the normal samples are at 0.28um.

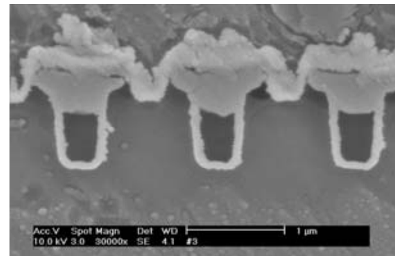

Figure 9 the cross section of the failure

4. Conclusion

From the failure mechanisms of gate resistance, the optimization can be done to upgrade the device's performance and reliability. This includes the fabrication process of the poly gate, the ohm contact of the poly gate and the metal bus line, the interface quality, the etching process control and the package process. All of these can be optimized with improved process to make the power DMOS with better switching performance, lower conduction resistance RDS(on) and better ruggedness under high thermal and electrical stress.

Acknowledgments

Fairchild Suzhou offers the intern opportunity.

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