A Performance Comparison of Dickson and Fibonacci Charge Pumps

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***Abstract*—This paper presents an analysis of two types of integrated charge pumps, Dickson and Fibonacci. The two circuits are compared in slow-switching conditions and at equal area occupation. A formula is developed for optimizing the capacitor sizes and improving the performance of the Fibonacci charge pump. The performance is evaluated with focus on voltage gain and output resistance and including the effects of parasitic capacitances.**

***Index Terms*—Voltage multiplier, charge pump, output resistance.**

I. Introduction

ON-CHIP generation of high voltages using only switches and capacitors is needed in many MOS-based systems like Flash memories. In such systems, two-phase DC-DC converters called charge pumps (CPs) transfer charge packets through a chain of capacitors from the power supply at a voltage V_{DD} to a load at a higher voltage V_{OUT}. The gain (G) is the ratio between the maximum open-circuit output voltage V_{OUT} and the input voltage V_{DD}. As power-supply voltages are progressively scaled down, designers strive to obtain higher gains without compromising energy efficiency or increasing area occupation. Hence, besides the popular Dickson CPs [1], it makes sense to explore alternate topologies such as Fibonacci CPs [2], which ideally are the two-phase CPs with the highest gain for a given number of capacitors [3], but are affected by non-idealities in monolithic implementations [4].

Since required gain and available silicon area are critical constraints for a designer, we decided to study how Dickson and Fibonacci CPs perform in conditions of equal gain and equal total area occupied by capacitors (which is the largest portion of an integrated CP). We assumed slow-switching conditions, where the switching period is much larger than the time constants due to capacitors and resistances of switches and sources. Under these conditions, we evaluated the CP performance in terms of equivalent output resistance R_{OUT}, which in turn has an impact on energy efficiency. Therefore, in this paper, we discuss the trade-off between gain and output resistance for a given area, we show how to optimize the output resistance of Fibonacci CPs, and we compare Dickson and Fibonacci CPs in the case of ideal capacitors and switches. Finally, we introduce the effect of parasitic capacitances and we present results from theoretical analysis and numerical simulations.

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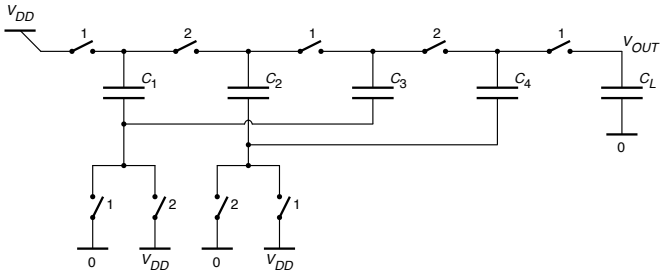

Fig. 1. Schematic diagram of a 4-stage Dickson CP ($N = 4$, $G = 5$).

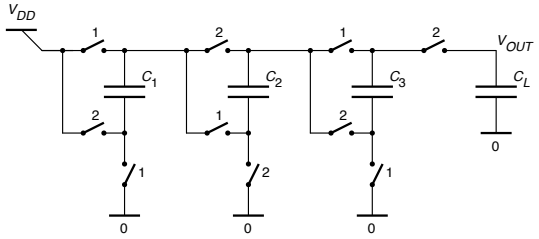

Fig. 2. Schematic diagram of a 3-stage Fibonacci CP ($N = 3$, $G = 5$).

II. Dickson and Fibonacci Circuits

In the Dickson CP in Fig. 1, when the switches are driven by two non-overlapping clock phases, each transfer capacitor (C_1 to C_4) is charged to the voltage of the preceding stage and then boosted by V_{DD} to charge the next stage at a higher voltage. If non-idealities are neglected, the steady-state voltage increment of each stage is V_{DD} and the resulting voltage gain of a CP with N stages is $G = N + 1$.

On the other hand, the Fibonacci CP in Fig. 2 achieves the same gain as the one in Fig. 1 with fewer capacitors. In general, this two-phase CP topology has the maximum attainable gain for a given number of capacitors [3]. Each transfer capacitor (C_1 to C_3) is charged to the voltage of the preceding stage and then boosted by the voltage of the preceding stage increasing the voltage of the next stage. As a result, the ideal voltage gain of a Fibonacci CP with N stages is $G = F_{N+1}$, where F_N is the N-th Fibonacci number, with $F_0 = F_1 = 1$ and $F_i = F_{i-1} + F_{i-2}$ for $i > 1$.

When a CP is connected to a load that dissipates power, its average output voltage drops to $V_{OUT} = G\ V_{DD} - R_{OUT}\ I_{OUT}$ because of the non-zero output resistance and the average load current I_{OUT}. At the same time, the CP energy efficiency is affected by the resistive losses given by $P_R = R_{OUT}\ I_{OUT}^2$. In the next section, we compare the output resistance of Dickson and Fibonacci CPs without non-idealities.

III. Trade-off Between Output Resistance and Gain

In the case of ideal linear elements, the procedure for evaluating the output resistance involves turning off the inputs (V_{DD}), applying an ideal source to the output, and calculating the ratio between voltage and current of the applied source [5]. In a two-phase circuit with switches and capacitors the output resistance [6] is given by

$$R_{OUT} = \frac{1}{f_s} \cdot \sum_{i=1}^{N} \frac{(a_{ci})^2}{C_i} , \quad (1)$$

where f_s is the switching frequency, N is the number of capacitors, C_i is the value of capacitor i, and $a_{ci} = q_i / q_{OUT}$ is its charge multiplier factor, which is the ratio of the charge q_i, transferred by capacitor C_i in a semi-period, and the charge q_{OUT} delivered to the load. The charge multiplier factors are calculated by applying KCL to the circuit in phase 1 and 2, and by considering that in steady state each capacitor receives and delivers the same charge in each of the two phases.

The charge multiplier factors for an N-stage Dickson CP are $a_{ci} = 1$ for $i = 1$ to N, therefore the output resistance is

$$R_{OUT} = \frac{1}{f_s} \cdot \sum_{i=1}^{N} \frac{1}{C_i} . \quad (2)$$

If the available silicon area is given, then the sum of the capacitances $C_T = C_1 + \ldots + C_N$ is a constant for the designer. In this case, the minimum (i.e. optimal) output resistance is obtained [7] when the value of each capacitor is

$$C_i = \frac{C_T}{N} . \quad (3)$$

Under these conditions, the output resistance is inversely proportional to the frequency f_s and to the total capacitance C_T, while it grows quadratically with the gain G, as shown by the formula below (with $G > 1$).

$$R_{OUT} = \frac{(G-1)^2}{f_s C_T} \quad (4)$$

In the case of an N-stage Fibonacci CP, the charge multiplier factors are $a_{ci} = F_{N-i}$ for $i = 1$ to N, therefore the output resistance is

$$R_{OUT} = \frac{1}{f_s} \cdot \sum_{i=1}^{N} \frac{(F_{N-i})^2}{C_i} . \quad (5)$$

If we consider a total capacitance C_T and equal stage capacitances given by C_T / N, the Fibonacci output resistance (5) grows faster than the Dickson's (2) when the gain increases. As an example, if we choose $f_s = 20$ MHz and $C_T = 100$ pF, the trade-off between gain and output resistance is shown in Fig. 3. The Fibonacci CP has the same output resistance as the Dickson's for $G = 2$ and $G = 3$ (since the circuits are equivalent), while it has a progressively larger output resistance at $G = 5$ ($N = 3$), $G = 8$ ($N = 4$), $G = 13$ ($N = 5$), and so on. Therefore, the Dickson CP has a better performance in these conditions. In the next section, we show how to select the values of the capacitors of the Fibonacci CP for minimizing its output resistance.

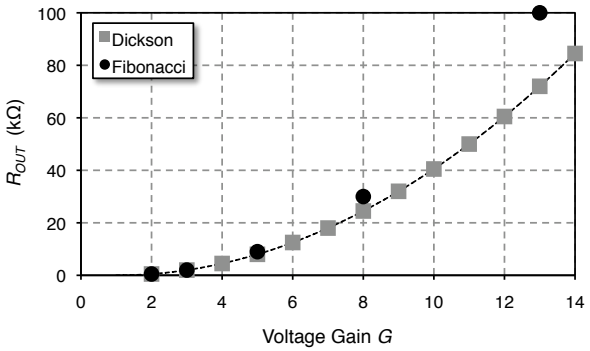

Fig. 3. Output resistance of Dickson and Fibonacci CPs as function of the gain, when $f_s = 20$ MHz, $C_T = 100$ pF, and when capacitors are equally sized.

IV. Optimization of the Fibonacci Output Resistance

To minimize the output resistance of the Fibonacci CP for a constant total capacitance C_T, we substitute $C_1 = C_T - C_2 - \ldots - C_N$ in (5) and we set the partials with respect to capacitors C_i equal to zero, which means

$$\frac{\partial R_{OUT}}{\partial C_i} = \frac{1}{f_s} \cdot \left(\frac{(F_{N-1})^2}{(C_T - C_2 - \ldots - C_N)^2} - \frac{(F_{N-i})^2}{C_i^2} \right) = 0 \quad (6)$$

for $i = 2$ to N, and leads to

$$C_i = \frac{C_T}{F_{N+1} - 1} \cdot F_{N-i} . \quad (7)$$

Therefore the optimal performance of an N-stage Fibonacci CP is not obtained when capacitances are equal (as in previous literature), but when they scale as the Fibonacci sequence with the largest capacitor next to V_{DD} and the smallest next to the load. Fig. 4 shows examples of optimal capacitor sizes.

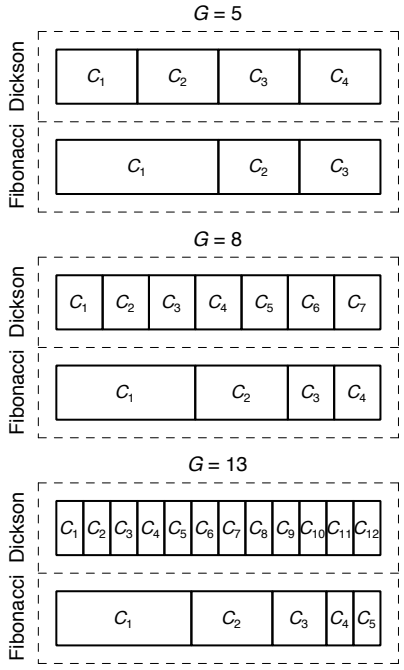

Fig. 4. Sketch of capacitors with optimal size for Dickson and Fibonacci CPs of equal area and gain (i.e. top $G = 5$, centre $G = 8$, bottom $G = 13$).

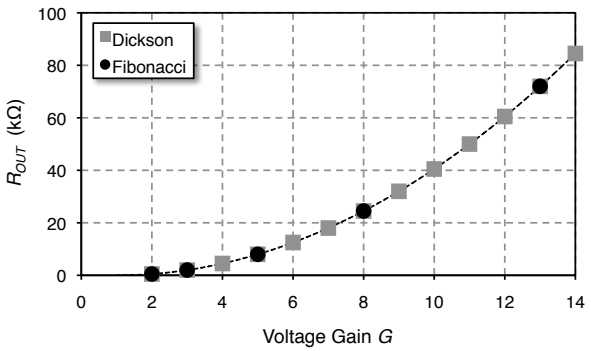

Fig. 5. Output resistance of Dickson and Fibonacci CPs as function of the gain, when f_s = 20 MHz, C_T = 100 pF, and when capacitors are optimized.

In the condition of equation (7), the Fibonacci CP has the same trade-off between gain and output resistance as the Dickson CP with equally-sized capacitors and same area. This trade-off corresponds to (4) and is shown in Fig. 5. As a result, the two CPs have equal performance in these conditions. As an example, for a given switching frequency f_s and a total capacitance C_T, at $G = 5$, $R_{OUT} = 16 / (f_s C_T)$ for both; at $G = 8$, $R_{OUT} = 49 / (f_s C_T)$ for both; and at $G = 13$, $R_{OUT} = 144 / (f_s C_T)$ for both.

V. Analysis with Parasitic Capacitances

One of the reasons why the performance of a real integrated CP deviates from the ideal is the unavoidable presence of parasitic elements modelled with a capacitor αC_i, connected between the bottom plate of C_i and the substrate, and with a capacitor βC_i, between the top plate of C_i and the substrate. When the top plate is a poly-silicon layer and the bottom plate is a diffused layer, typical values are $\alpha = 0.1$ and $\beta = 0.05$.

For the Dickson CP with parasitic elements [1] the gain is

$$G = \frac{N}{1+\beta} + 1 \,, \tag{8}$$

the output resistance for equally-sized capacitors is

$$R_{OUT} = \frac{N^2}{(1+\beta) f_s C_T} \,, \tag{9}$$

and the relationship between output resistance and gain is

$$R_{OUT} = \frac{1+\beta}{f_s C_T} \cdot (G-1)^2 \,. \tag{10}$$

The performance does not depend on α, because the circuit can be built so that the bottom plates of all capacitors are alternately connected to ground and V_{DD} without affecting the charge transfer through the CP.

To calculate the voltage gain of the optimized Fibonacci CP with parasitic elements we followed the method proposed in [4] and based on [8], which is convenient because the number of equations is the same as for the ideal case. Two matrixes represent the circuit topology in each switching phase, while two other matrixes contain the values of capacitors (including parasitic elements) and the values of voltage sources. Node voltages and gain are calculated through conservation laws.

By applying the method stated above, we calculated the analytical expressions of G as a function of α and β reported in Table I and the numerical values of G when $\alpha = 0.1$ and $\beta = 0.05$ listed in Table II. The gain with parasitic elements is lower than the ideal gain, because a portion of each charge packet transferred between stages is shared with the parasitic capacitors and wasted.

To evaluate the effect of parasitic elements on the output resistance, we turned off V_{DD}, connected a voltage source at the output, applied the method above one more time, and found the charge q_{OUT} delivered by the voltage source during the switching period, the corresponding current, and thus the output resistance. The analytical expressions are shown in Table I and the numerical values in Table II. The output resistance with parasitic elements is lower than the ideal, because it is inversely proportional to the node capacitances that increase with the parasitics.

Table III compares gain and output resistance of Fibonacci CPs with optimized capacitors and with equally-sized capacitors when parasitics are considered. The optimized CP has a better performance because the largest capacitors of the first two stages, which have the largest parasitics, are alternately connected to ground and V_{DD}.

TABLE I
Analytical Expressions of Gain and Output Resistance of Optimized Fibonacci CPs with Parasitic Capacitances

N	G	R_{OUT}
1	$\frac{2+\beta}{1+\beta}$	$\frac{1}{f_s C_T} \cdot \frac{1}{1+\beta}$
2	$\frac{3+\beta}{1+\beta}$	$\frac{1}{f_s C_T} \cdot \frac{4}{1+\beta}$
3	$\frac{\alpha(1+\beta)+(2+\beta)(5+2\beta(4+\beta))}{(1+\beta)(2+\alpha+(5+\alpha)\beta+2\beta^2)}$	$\frac{4}{f_s C_T} \cdot \frac{2\alpha(1+\beta)+(2+\beta)(4+5\beta)}{(1+\beta)(2+\alpha+(5+\alpha)\beta+2\beta^2)}$
4	$\frac{\left[\begin{matrix}48+\alpha(1+\beta)(8+5\beta)+\\+\beta(4+\beta)(35+6\beta(4+\beta))\end{matrix}\right]}{\left[\begin{matrix}(3+2\beta)(2+3\beta)(1+\beta(3+\beta))+\\+\alpha^2(1+\beta)^2+\alpha(1+\beta)(7+\beta(16+7\beta))\end{matrix}\right]}$	$\frac{7}{f_s C_T} \cdot \frac{\left[\begin{matrix}42+2\alpha^2(1+\beta)+\alpha(19+3\beta(12+5\beta))+\\+\beta(109+\beta(80+17\beta))\end{matrix}\right]}{\left[\begin{matrix}(3+2\beta)(2+3\beta)(1+\beta(3+\beta))+\\+\alpha^2(1+\beta)^2+\alpha(1+\beta)(7+\beta(16+7\beta))\end{matrix}\right]}$

TABLE II
Numerical Values of Gain and Output Resistance of Optimized Fibonacci CPs with Parasitic Capacitances

N	G ideal	G calculated	G simulation	R_{OUT} ideal	R_{OUT} calculated	R_{OUT} simulation
1	2	1.952	1.952	500 Ω	476.2 Ω	476.2 Ω
2	3	2.905	2.905	2 kΩ	1.905 kΩ	1.906 kΩ
3	5	4.514	4.514	8 kΩ	7.201 kΩ	7.204 kΩ
4	8	6.601	6.601	24.5 kΩ	20.46 kΩ	20.46 kΩ
5	13	9.119	9.119	72 kΩ	52.04 kΩ	52.05 kΩ
6	21	11.81	11.81	200 kΩ	118.2 kΩ	118.1 kΩ

The numerical values are calculated using the analytical expressions and then verified through Spectre simulations with ideal switches. The values correspond to $\alpha = 0.1$, $\beta = 0.05$, f_s = 20 MHz, and C_T = 100 pF.

TABLE III
GAIN AND OUTPUT RESISTANCE OF FIBONACCI CPS WITH EQUALLY-SIZED CAPACITORS AND WITH OPTIMIZED CAPACITORS

N	G equally-sized	G optimized	R_{OUT} equally-sized	R_{OUT} optimized
1	1.952	1.952	476.2 Ω	476.2 Ω
2	2.905	2.905	1.905 kΩ	1.905 kΩ
3	4.294	4.514	7.631 kΩ	7.201 kΩ
4	5.498	6.601	20.77 kΩ	20.46 kΩ
5	5.560	9.119	43.82 kΩ	52.04 kΩ
6	4.504	11.81	70.19 kΩ	118.2 kΩ

The values correspond to $\alpha = 0.1$, $\beta = 0.05$, $f_s = 20$ MHz, and $C_T = 100$ pF.

Since the parasitic elements reduce both the gain and the output resistance of the Dickson and the optimized Fibonacci CPs, we compared the two CPs by considering the R_{OUT}-G trade-off shown in Fig. 6. The Dickson CP has a better performance than the Fibonacci CP when $G > 3$, because the Dickson output resistance is lower at any given gain.

Fig. 7 shows an example of current-voltage characteristic of the two CPs with parasitic capacitors. The 4-stage Dickson CP has a gain $G = 4.8$ and an output resistance $R_{OUT} = 7.6$ kΩ; the 3-stage Fibonacci CP has a lower gain $G = 4.5$ and a lower output resistance $R_{OUT} = 7.2$ kΩ; and finally the 3-stage Dickson CP has a gain $G = 3.9$ and an output resistance $R_{OUT} = 4.3$ kΩ.

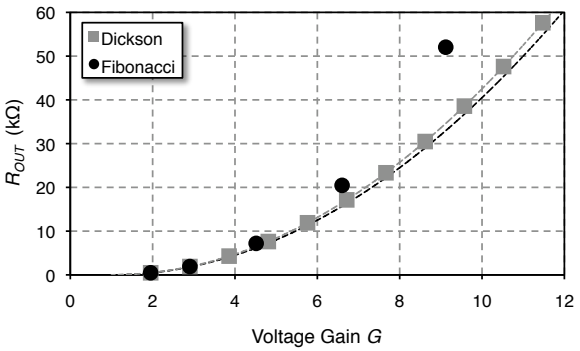

Fig. 6. Impact of parasitic capacitances on the R_{OUT}-G trade-off of the Dickson CP and the Fibonacci CP with optimized capacitors when $\alpha = 0.1$, $\beta = 0.05$, $f_s = 20$ MHz, and $C_T = 100$ pF.

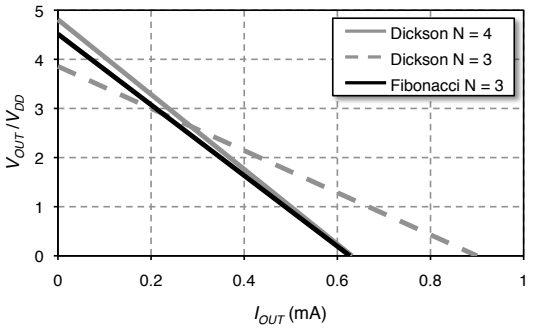

Fig. 7. Output voltage as a function of output current I_{OUT} with parasitic capacitance for Dickson CPs with $N = 3$ and $N = 4$ and Fibonacci CPs with $N = 3$ when $\alpha = 0.1$, $\beta = 0.05$, $f_s = 20$ MHz, and $C_T = 100$ pF.

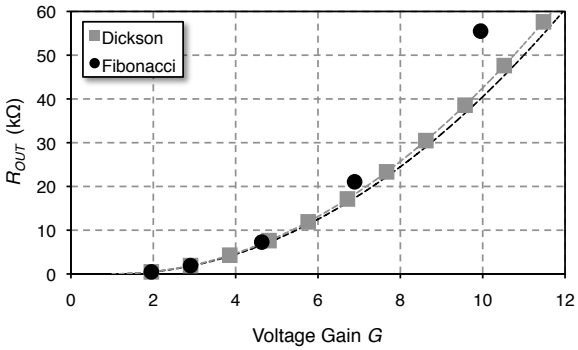

Fig. 8. Impact of parasitic capacitances on the R_{OUT}-G trade-off of the Dickson CP and the Fibonacci CP with optimized capacitors when $\alpha = \beta = 0.05$, $f_s = 20$ MHz, and $C_T = 100$ pF.

The Dickson CP has a better performance also if we assume $\beta = 0$ or $\alpha = \beta$. As an example, the R_{OUT}-G trade-offs when top and bottom plate parasitics are the same (i.e. $\alpha = \beta = 0.05$) is shown in Fig. 8. The reduction of the bottom-plate parasitic capacitance results in an increased gain of the Fibonacci CP. The performance of the two CPs is closer at $G = 5$, while at higher gains the performance of the Dickson CP is still better.

VI. CONCLUSION

In this paper, we presented a comparison of Dickson and Fibonacci CPs. We derived a simple formula to optimize the capacitor sizes of the Fibonacci CP. Then we compared the optimized Fibonacci CP with the Dickson CP by considering the trade-off between output resistance and gain in slow-switching conditions and at equal area occupation. We showed that in ideal conditions the two CPs have the same performance, while the Dickson CP has a better performance when parasitic capacitances are included, especially for high gains. However, the optimization of the capacitor sizes makes the Fibonacci CP more competitive. The simulation results are in good agreement with the presented analytical description that can facilitate the choices of the designer.

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