Duty Cycle Correction Using Negative Feedback Loop

An analog solution

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Abstract— **An architecture has been proposed to attain a duty cycle of nearly 50% for single ended signals. The main idea is based on the fact that the average DC value of a signal is proportional to its Duty Cycle. So, if we assure that a signal and its inverted counterpart have equal average DC value, that particular signal will have a 50% duty cycle. A feedback circuit is used to compare the average DC values and correct the duty cycle of the signal. The duty correction circuit was implemented in 130nm technology with a power supply of 1.2V. It was found by simulation that the circuit gives nearly 50% duty cycle at the output for a 500MHz signal when the input duty cycle is varied from 25% to 75%.**

Index Terms— ***Duty cycle*, analog solution, feedback.**

I. INTRODUCTION

Duty cycle distortion is introduced by device mismatches, process imbalance, etc. Duty cycle becomes an important specification when there is a minimum (or maximum) constraint on the pulse width. One of those situations is when the signal has to be sampled by a clock at the receiver, during the valid data window. During such a situation, it should be ensured that the data signal is wide enough to be sampled in the valid data window to prevent distortions. There are several digital implementations for duty cycle correction. One of them has been explained in [1]. In this approach the duty correction circuit has been included in the DLL loop itself, but such an implementation might affect the working of the loop and may add jitter. Moreover, the circuitry and working is quite complex. In this paper, an analog solution has been proposed in which a negative feedback loop has been used for duty cycle correction. The loop settles within 1us after enabling the circuit. There is no necessity of a reference voltage as the reference is generated using the signal itself. Also, because the correction circuit can be isolated from the PLL/DLL loop, it doesn't affect the working of the clock circuits.

For high frequency signals (of about 2.5GHz), a method proposed in [2] may be utilized. But for medium frequency signals (500MHz to 1GHz), the simple method proposed in this paper can be utilized, though experimentations are going on to make the proposed circuit work satisfactorily at very high frequencies.

The working of the proposed duty correction circuit and its block diagram has been explained in section II. The results of simulation have been summarized in section III. Section IV contains the conclusion and future work needed to improve the performance.

II. PROPOSED ARCHITECTURE

Fig. 1 shows the proposed architecture for duty cycle correction. It has the following blocks: Average value detector, Comparator and Duty-alter block. V_{Err} is adjusted until V_A and V_B are equal, by the action of the feedback loop and the comparator. The subsequent sections describe the configuration of the mentioned blocks.
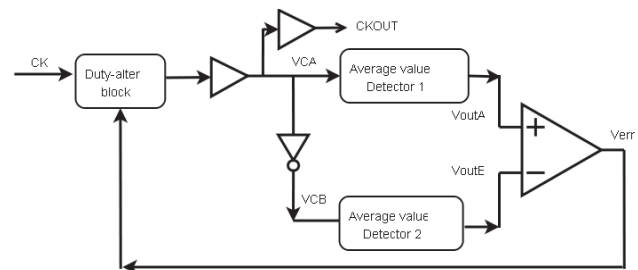

Figure 1. Block diagram of the proposed architecture

A. Proposed Average Value Detector

The average value detector is basically a low pass filter which filters out the high frequency components and retains the average DC value of the signal. The simple architecture that was used for the purpose is shown in Fig. 2. The working has been explained below:

When V_{CA} is high, M1 is ON and the current I_{DC} flows to ground. When V_{CA} is low, M1 is OFF and the current I_{DC} flows through the RC circuit and charges C_1 to V_{outA}.

Consider the charge Q accumulated across the capacitor C_1, given by

$$Q = C_1 * V_{outA} \qquad (1)$$

But $\quad Q = I_{DC} * T_{OFF} \qquad\qquad (2)$

From (1) and (2) we have,

$$I_{DC} * T_{OFF} = C_1 * V_{out}$$

Or $\quad V_{outA} = (I_{DC} * T_{OFF}) / (C_1) \qquad (3)$

V_{outA} is proportional to T_{OFF}

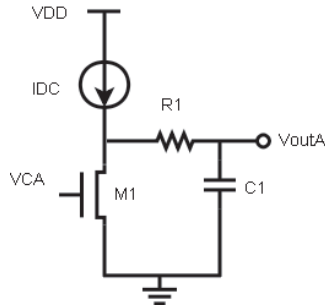Similarly, $V_{outB} = (I_{DC} * T_{ON}) / (C_1) \qquad (4)$

Figure 2.   Schematic of average value detector

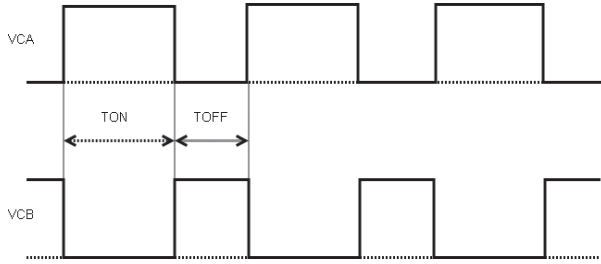The waveforms of V_{CA} and V_{CB} can be referred from Fig. 3.

Figure 3.   Waveforms of V_{CA} and V_{CB}

Experimentation is going on with alternative circuit for average value detector. A circuit which is similar to a charge pump, shown in Fig. 4 is found to provide duty correction over a range of frequencies (200MHz to 1 GHz) but the loop is not stable at low input duty cycle (30%) at FF corner. So, currently work is going on to improve the stability of the loop.
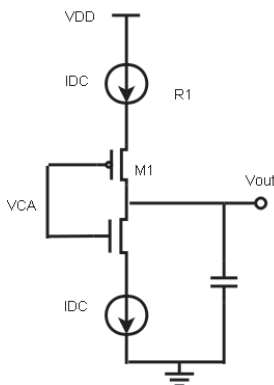

Figure 4.   Alternative circuit for Average detector

Apart from limited frequency range, the performance of the average value detector is limited by the current mismatch between the two detectors. The LHS in (3) and (4) are equal only if I_{DC} is equal. Therefore, if there is a mismatch between I_{DC} in the two average value detectors, V_{outA} and V_{outB} are not equal and hence 50% duty cycle cannot be assured at the output.

B. Proposed Comparator

The comparator is an opamp which has V_{outA} and V_{outB} as inputs and V_{Err} as output. V_{Err} is fed back to the Duty-alter block which adjusts the duty cycle by keeping V_{outA} and V_{outB} nearly equal.

From equations (3) and (4) we have $T_{ON} = T_{OFF}$, if we assure that $V_{outA} = V_{outB}$, which can be assured by the action of the opamp with negative feedback. Therefore, if $T_{ON} = T_{OFF}$, we have a signal with 50% duty cycle at the output.

Care should be taken to design the opamp such that there is no systematic offset between the inputs of the opamp. Offset between the inputs also results in non-50% duty cycle at the output. Also, opamp with high open loop gain gives a good performance.

C. Proposed Duty-Alter block

The structure of the "Duty-alter" block is shown in Fig. 4. Output of the opamp is connected to the gate of the NMOS and the signal whose duty is to be corrected is connected to the gate of the PMOS as shown. The duty cycle of the signal produced at the output is inversely proportional to V_{Err} (when is $V_{Err} > V_{Thn}$). By changing the value of V_{Err}, we can change the duty cycle of the output signal. Therefore, by the action of the feedback loop, V_{Err} is adjusted such that 50% duty cycle is achieved.
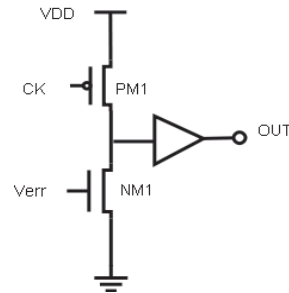

Figure 5.   Circuit for "Duty-alter" block

III.   SIMULATION RESULTS

In order to confirm the validity of the proposed ideas and to evaluate the performance, the duty correction circuit was implemented in TSMC 130nm technology and simulated using BSIMv3 models. Power supply voltage is 1.2V (typical). The input signal with various duty cycle values was given using a signal generator. The frequency of the signal was set to 500MHz. The circuit requires calibration (for R and C in the low pass filter) for very low frequency signals.

The circuit was tested across 3 corner conditions with 9 input duty conditions. The results have been summarized using the plots in Fig. 5. It can be observed from the figure that when the input duty cycle is varied +/50% (i.e. 25% to 75%) the output duty cycle varies by about +/-1%.

Fig. 6 shows the settling behavior of V_{outA}, V_{outB} and V_{Err} at FF corner, 1.32 V and -40 C. It can be observed from the waveforms that there are no stability issues with the feedback loop.
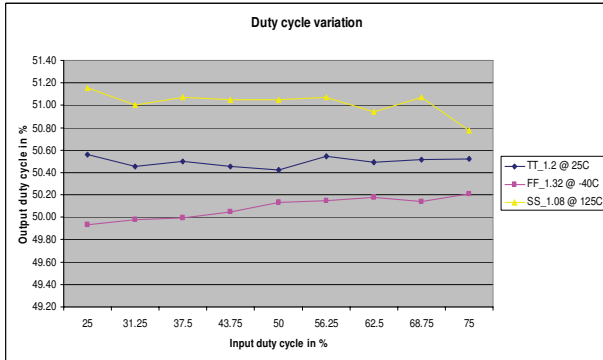

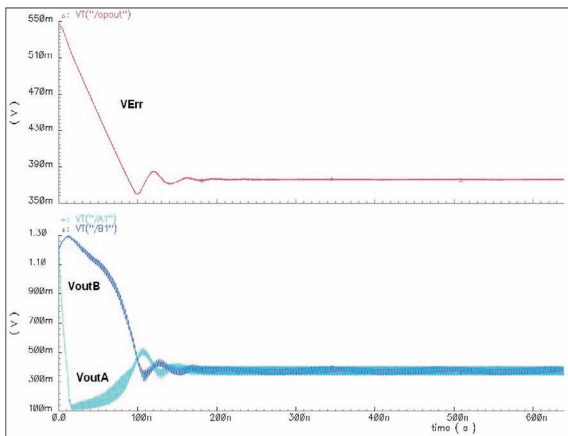Figure 6. Variation of output duty cycle

Figure 7. Settling behavior of inputs and output of the opamp

The circuit was tested by changing the duty cycle on the fly to check the response of the loop. The result is plotted in Fig. 8. We can observe that the control voltage V_{Err} settles to a stable value within about 50 cycles. The figure shows the V_{Err} waveform for input ON time of 1.3ns, 1.2ns and 1.1ns (i.e. for input duty of 65%, 60% and 55% respectively).
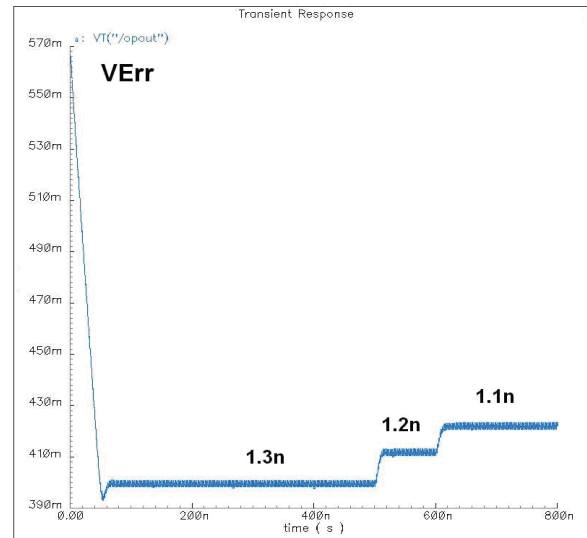

Figure 8. Settling behavior of V_{Err} for different input duty cycles

IV. CONCLUSION

A duty cycle correction circuit has been proposed and demonstrated using analog blocks with a negative feedback loop. The circuit can be implemented using simple blocks as demonstrated, providing an output duty cycle of close to 50%.

The performance of the circuit can be improved by modifying the "Duty-alter block" and the low pass filter. Future work includes modifying the "Duty-alter block" to make it more robust and reduce the current consumption. Also, the low pass filter uses bulky capacitors and resistors which can hopefully be replaced by more area-efficient implementations in the future.

REFERENCES

[1] Keun-Soo Song, Cheul-Hee Koo, Nak-Kyu Park, Kwan-Weon Kim,Young-Jung Choi, Jin-Hong Ahn, Byong-Tae Chung, "A Single-Loop DLL Using an OR-AND Duty-Cycle Correction Technique," Proceedings, IEEE Asian Solid-State Circuits Conference, Nov 2008.

[2] Kazuyuki Nakamura, Muneo Fukaishi, Yoshinori Hirota, Youetsu Nakazawa and Michio Yotsuyanagi, "A CMOS 50% Duty Cycle Repeater Using Complementary Phase Blending", 2000 Symposium on VLSl Circuits Digest of Technical Papers.