Single supply high PSRR class AB amplifier

M. Loikkanen, P. Keränen and J. Kostamovaara

A simple two-stage Miller compensated class AB amplifier is presented which uses single-ended class AB control for accurate setting of the output stage quiescent and minimum currents. This control technique also inherently boosts the amplifier midband positive power supply rejection ratio ($PSRR_{dd}$). Measurements show a more than 20 dB improvement in the midband $PSRR_{dd}$ when the amplifier is compared to popular symmetrical class AB amplifiers with similar bandwidth.

Introduction: Modern-day analogue blocks have to operate in a hostile system-on-a-chip environment in which power supplies are corrupted by switching noise from digital logic and other switching circuits. This can lead to a reduction in the dynamic range of the whole system, especially in high precision systems or if the circuits that are sensitive to supply noise are at the very beginning of the power supply/reference chain. It is therefore essential that the circuits in these applications, e.g. operational amplifiers that are used as voltage reference buffers or as on chip low dropout regulators, have good positive power supply regulation not only at DC but also at high frequencies [1, 2]. When aiming at good $PSRR_{dd}$ performance above the dominant pole frequency of the amplifier, one should be able to lower the positive power supply gain at these frequencies. Unfortunately, when the compensation network is applied symmetrically across the amplifier output stage, the attenuation is only −6 dB, which makes the $PSRR_{dd}$ of these amplifiers track the open loop gain plot closely. It should be noted that this behaviour is due to the symmetrical compensation network and not due to the chosen compensation strategy.

Several possibilities exist for improving the midband $PSRR_{dd}$. One is to use cascode compensation and apply the compensation network only across the NMOS output stage [3]. However, when the amplifier has to be able to source/sink large currents, a symmetrical compensation network with Miller compensation is nevertheless preferred [4], because this allows better control over a possibly poorly damped complex pole pair. When Miller compensation is used $PSRR_{dd}$ can be improved by using published techniques such as in [5] or [6]. From the point of view of maximum obtainable signal bandwidth, required additional silicon area, and quiescent current efficiency, these techniques are equally good. When high DC gain is needed, however, [6] is preferred due to its gain boosted amplifier topology.

This Letter introduces a low voltage compatible $PSRR_{dd}$ improvement technique for class AB amplifiers, which does not increase silicon area or limit amplifier bandwith. The technique is based on a ground referenced class AB control circuit which explicitly controls only the PMOS side output stage transistor while relying on global feedback around the amplifier for the control of the NMOS side.

Circuit description: The circuit, shown in Fig. 1, is a modified version of the class AB amplifier described in [7]. The major differences relative to the original circuit are: (i) inclusion of the thick gate oxide transistor M6HV, which shields the NMOS cascode transistors from impact ionisation at high supply voltages, (ii) completely separated NMOS and PMOS side signal paths, and (iii) single-ended current mode class AB control for robust control of the output stage quiescent and minimum currents.

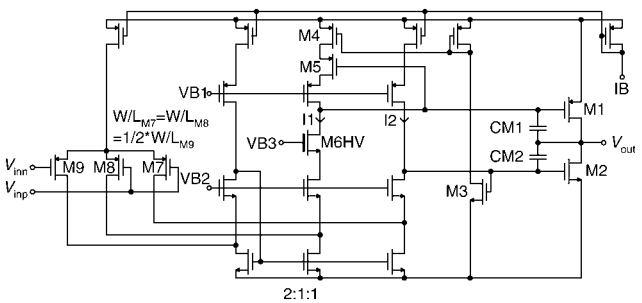

Fig. 1 *Schematic diagram of amplifier*

The local class AB feedback loop explicitly controls only the biasing of the PMOS output stage. In Fig. 1 quiescent point M4 operates in the triode region and M5 in the active region, therefore the class AB operation at the quiescent point and when the NMOS output stage is sinking current is the same as in [7]. The control of the NMOS output stage minimum current when the PMOS side is sourcing current is different, however, as it relies on the resistive feedback path around the amplifier.

To see why M2 minimum current is also well controlled when M1 is sourcing current, consider what would happen if M2 were driven to cut off. This would also drive M4 into cut off, which would in turn pull M1 gate all the way to ground. This is not permitted by the global feedback around the amplifier, which forces I1 to be equal to I2, and so M2 always stays on minimum current, which is approximately 0.5 times the quiescent current value.

Using a class AB control loop to boost amplifier midband $PSRR_{dd}$: The main idea behind the $PSRR_{dd}$ improvement technique discussed here is to use ground referenced negative feedback, provided by the class AB control loop, to lower the positive power supply gain (A_{dd}) above the dominant pole frequency. The negative feedback path that is responsible for boosting $PSRR_{dd}$ can be most easily seen by looking at the small signal model of the output stage as shown in Fig. 2. By assuming first that V_{out} disturbance is small; we can discard $gm2$ for a while. Now it is easy to see that $gm3$ together with $gm1$ create a ground referenced Miller compensated amplifier which has a feedback network formed by $CM2$ and $R2$ around it. It is this feedback that attenuates any disturbance injected from the power supply through $gm1$ by the frequency dependent loop gain.

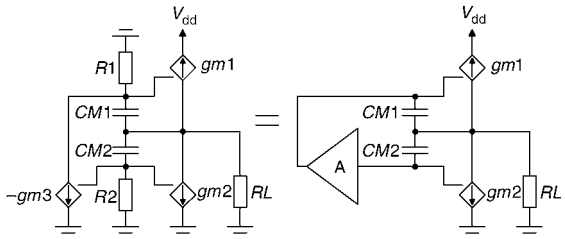

Fig. 2 *Small signal model for calculating A_{dd}*

Complete analysis of the small signal model results in (1), where it is assumed for simplicity that $R1 = R2$ and $CM1 = CM2$:

$$A_{dd}(s) = \frac{V_{out}(s)}{V_{dd}(s)} = \frac{gm1RL\ (1 + 2CM1R2s + CM1^2R2^2s^2)}{(1 + gm1gm3R2^2RLCM1s)(1 + ((CM1(gm1 + gm2))/(gm1gm3)))} \quad (1)$$

At midband frequencies, (1) can be further simplified to

$$A_{dd}(s) = \frac{V_{out}(s)}{V_{dd}(s)} = \frac{(1 + CM1R2s)^2}{gm3R2^2CM1s} \quad (2)$$

Equation (2) shows that the amplifier maintains its DC $PSRR_{dd}$ performance up to the double zero frequency, which results in a maximum attenuation of

$$Attenuation_{max} = 20\log(gm3R2) \quad (3)$$

which can be as much as 40 dB more than that obtainable from symmetrical class AB stages. As shown in Table 1, midband attenuation also remains good when the NMOS output stage is on minimum current, even though the zero locations given by (2) are slightly changed.

Table 1: Typical measured performance of amplifier

Supply range	2.7–5 V
Typical load	20 pF‖1 MΩ
Quiescent current consumption	165 μA
DC gain	>90 dB
Unity gain frequency and phase margin	5.4 MHz, 61°
$1/PSRR_{dd}$ at 100 kHz, $I_{out} < I_{quiescent}$	−64 dB
$1/PSRR_{dd}$ at 100 kHz, $I_{out} = 0.4$ mA	58 dB

Measurement results: The amplifier was manufactured in a high voltage 0.35 μm CMOS process. A typical measured large signal pulse response with heavy resistive and capacitive load is shown in Fig. 3. The fact that there are no sustained oscillations in the Figure prove the stability of the

class AB loop also when one of the output stage transistors is on minimum current. Typical measured and simulated $1/\mathrm{PSRR_{dd}}$ performances of the amplifier and a simulated response of an amplifier with a Monticelli-type [8] symmetrical class AB output stage are shown in Fig. 4, which clearly indicates the benefits of using single-ended class AB control when the power supply contains high frequency disturbances within the operating bandwidth of the amplifier. Other aspects of the performance of the amplifier are summarised in Table 1.

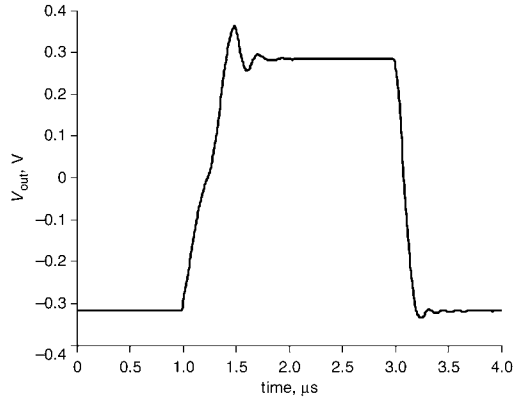

Fig. 3 *Large signal pulse response of amplifier with 50 pF‖100 Ω load*

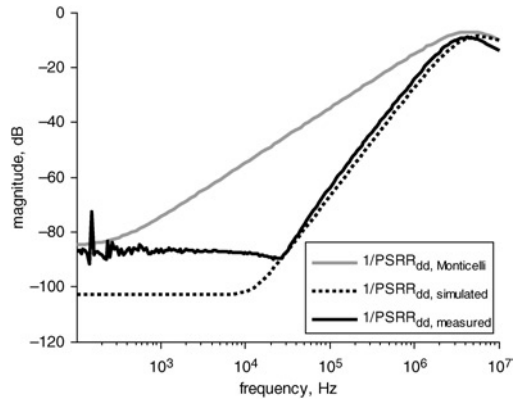

Fig. 4 *Comparison of measured $1/PSRR_{dd}$ with simulations and with amplifier having standard symmetrical class AB output stage*

Conclusion: The theory and measurements presented here demonstrate that single-ended current mode class AB control allows robust control of the amplifier output-stage quiescent and minimum currents, and in addition inherently improves its midband $\mathrm{PSRR_{dd}}$ performance.

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