PSRR improvement technique for single supply class AB power amplifiers

M. Loikkanen, G. Bognár and J. Kostamovaara

A simple circuit technique for improving the midband positive power supply rejection ratio ($PSRR_{dd}$) of gain boosted class AB power amplifiers is presented. The technique takes advantage of the bias network and inherent narrow gain boosting amplifier bandwidth and therefore does not require any additional components. Measurements show that more than 20 dB improvement in the midband $PSRR_{dd}$ is obtainable at a frequency of 100 kHz.

Introduction: The low supply voltages of modern IC processes place stringent limitations on the attainable dynamic range of analogue signal processing blocks such as operational amplifiers [1]. In certain buffer and audio applications, where the heavy resistive load is ground referenced, so that differential signal processing is not easily applicable, the dynamic range can be limited among noise and nonlinearities by the limited midband $PSRR_{dd}$. This is especially the case when a non-unity gain amplifier is operated in a single supply, mixed signal environment, where the extensive use of switching regulators and digital logic normally calls for some kind of power supply pre-regulation [2].

Although a huge number of compensation techniques have been published to date, the most common and preferred way of stabilising a power amplifier is still two-stage Miller compensation (SMC) [3, 4]. Two principal problems arise when SMC is used with the popular class AB output stages [5, 6]. First, because the Miller capacitance acts as a short circuit after the dominating pole, the output stage behaves like a non-inverting unity gain amplifier, and thus the positive supply noise is attenuated only by the frequency-dependent loop gain (LG) [7]. Secondly, the symmetry of the mentioned class AB structures causes the $PSRR_{dd}$ to be approximately equal to the negative supply rejection ratio ($PSRR_{ss}$). Note, however, that in single supply applications it is $PSRR_{dd}$ that is of concern, because the lower supply rail of the amplifier is normally connected to the ground node by default.

This Letter introduces a $PSRR_{dd}$ improvement circuit technique for two-stage Miller compensated gain boosted power amplifiers that use feedback type class AB biasing [5]. The technique is based on creating an additional cancelling signal path in an asymmetrical manner from the power supply to the output using a bias network and local gain boosting amplifier bandwidth limiting capacitance. It utilises efficiently already existing circuit components and therefore does not increase the amplifier quiescent current consumption, unlike [8]. Also, the suggested technique does not influence the amplifier stability margins, which gives it a clear advantage over $PSRR_{dd}$ improvement techniques presented in [9, 10].

Circuit description: The amplifier, shown in Fig. 1, is a modified version of a circuit described in [5]. The DC gain of the basic structure has been improved by connecting two current input gain boosting amplifiers, shown in Fig. 2, to the split cascode transistors. High voltage operation is improved by adding a thick gate oxide transistor M4HV, which shields M15 from impact ionisation. Quiescent current stability is improved by adding a V_{DS} stabilising transistor M5HV on top of the current measurement transistor M10 and by adding transistors M8 and M9, which create a supply-dependent bleeding current path which compensates for the supply dependent change in VB2, thus keeping the current in the class AB circuit (M10-M14) constant.

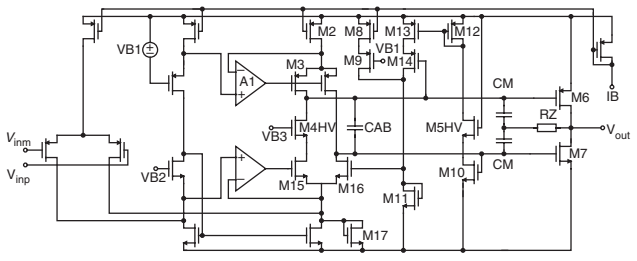

Fig. 1 *Simplified schematic diagram of amplifier*

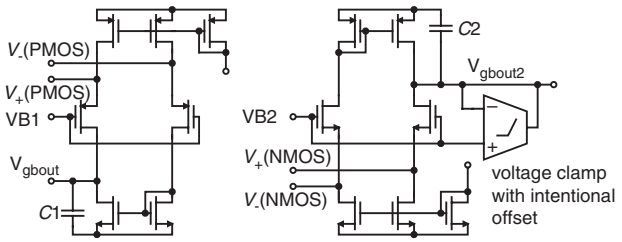

Fig. 2 *Upper and lower gain boosting amplifiers of Fig. 1*

PSRR improvement technique: The basic principle of the PSRR improvement technique discussed here is to generate an additional parallel signal path with a gain of −1 from the positive power supply to the output, which cancels the unity gain signal path through the output stage in an asymmetrical manner above the dominant pole frequency. The asymmetry is obtained by applying transconductance-output impedance matching, which is explained in the following, only to the PMOS side.

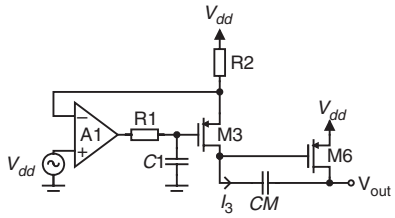

Fig. 3 *Half-circuit for calculation of A_{dd}*

The mechanism by which the additional signal path is created can be easily understood by analysing the positive power supply gain (A_{dd}) half-circuit shown in Fig. 3. In this Figure $R1$ is the output impedance of the PMOS side gain boosting amplifier, of which positive input sees the full power supply disturbance through the bias network. $C1$ is a capacitance used to limit the gain boosting amplifier bandwidth and $R2$ is the output impedance of the transistor $M2$ seen in Fig. 1.

Solving the transfer function $I_3(s)/V_{dd}(s)$ from Fig. 3, we obtain

$$\frac{I_3(s)}{V_{dd}(s)} = \frac{(1/(R2 \times A1))(1 + R1 \times C1 \times s)}{1 + ((R1 \times C1 \times s)/A1)} \tag{1}$$

At midband frequencies (1) can be further simplified to

$$\frac{I_3(s)}{V_{dd}(s)} = \frac{R1 \times C1 \times s}{R2 \times A1} \tag{2}$$

Combining (2) with an approximate output stage transfer function

$$\frac{V_{out}(s)}{I_3(s)} = \frac{-1}{CM \times s} \tag{3}$$

results in a gain of −1 as long as

$$C1 = \frac{A1 \times R2 \times CM}{R1} = gm1 \times R2 \times CM \tag{4}$$

where $gm1$ is the gain boosting amplifier input stage transconductance, i.e. the technique relies on accurate matching of the two capacitors and a fixed $gm1 \times R2$ product to be effective. Complete analysis of Fig. 3 with the output stage reveals that the above choice, which sets the additional signal path gain to −1, creates two complex high frequency zeros, which appear approximately at

$$|z1, z2| = \sqrt{\frac{gm1 \times R1 \times R2 - R3}{C1 \times CM \times R1 \times R2 \times R3}} \tag{5}$$

Equation (5) is useful for design purposes, because the zero locations indicate the frequency up to which the amplifier maintains its DC power supply rejection performance.

Measurement results: The amplifier was manufactured in a high voltage 0.35 µm CMOS process. Typical measured power supply noise attenuation curves are shown in Fig. 4. At 100 kHz the measured $PSRR_{dd}$ was typically 63 dB over the measured temperature

range −40 to 85°C and supply range of 2.7 to 5 V, which is almost 20 dB higher than that obtainable from symmetrical class AB topologies. Other aspects of the amplifier performance are summarised in Table 1.

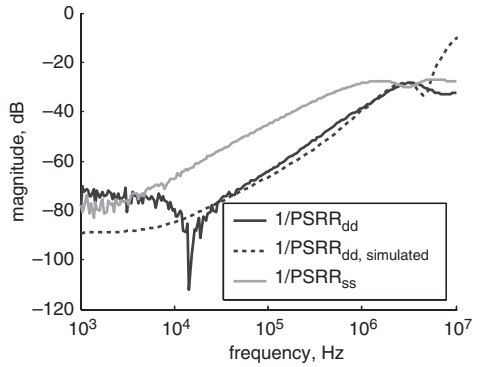

Fig. 4 *Measured and simulated PSRR performance*

Table 1: Typical amplifier performance

Supply range	2.7–5 V
Operating temperature range	−40–85°C
Typical load	20 pF‖10 kΩ
Quiescent current consumption	298 μA
DC gain	>106 dB
Maximum output current with 5Ω load	>109 mA
Unity gain frequency and phase margin	10.6 MHz, 51°
Slew rate min.	5.8 V/μs

Conclusion: The theory and measurements presented demonstrate how the power supply rejection ratio of single supply gain boosted class AB power amplifiers can be improved without additional components by utilising the existing bias network and narrow gain boosting amplifier bandwidth.

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References

1 Huijsing, J., Hogervorst, R., and de Langen, K.-J.: 'Low voltage low power amplifiers'. Int. Symp. on Circuits and Systems, 1993, Vol. 2, pp. 1443–1446
2 'Circuit refinements ensure quality audio in portable computers', 2004, Maxim application note no. 2980
3 Ivanov, V., and Filanovsky, I.: 'Operational amplifier speed and accuracy improvement: analog circuit design with structural methodology' (Kluwer Academic, Dordrecht, The Netherlands, 2004)
4 Loikkanen, M., and Kostamovaara, J.: 'Low voltage CMOS power amplifier with rail-to-rail input and output', *Analog Integr. Circuits Signal Process.*, 2006, **46**, (3), pp. 183–192
5 de Langen, K.-J., and Huijsing, J.: 'Compact low-voltage power-efficient operational amplifier cells for VSLI', *IEEE J. Solid-State Circuits*, 1998, **33**, (10), pp. 1173–1181
6 Monticelli, D.: 'A quad CMOS single-supply opamp with rail-to-rail output swing', *IEEE J. Solid-State Circuits*, 1986, **SC-21**, pp. 1026–1034
7 Laker, K., and Sansen, W.: 'Design of analog integrated circuits and systems' (McGraw-Hill Inc., Singapore, 1994)
8 Loikkanen, M., and Kostamovaara, J.: 'PSRR improvement technique for amplifiers with Miller capacitor'. Int. Symp. on Circuits and Systems pp. 1394–1397
9 Säckinger, E., Goette, J., and Guggenbühl, W.: 'A general relationship between amplifier parameters, and its application to PSRR improvement', *IEEE J. Solid-State Circuits*, 1991, **38**, (10), pp. 1173–1181
10 Whatley, R.: 'Circuit for improving power supply rejection in an operational amplifier with frequency compensation', 1987, US patent no. 4,713,625