Single-stage class AB operational amplifier for SC circuits

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A single-stage class AB multipath operational amplifier is presented. The proposed amplifier uses the previously idle devices in a folded-cascode amplifier in the signal path and a flipped-voltage follower cell to build the class AB operation. It results in enhanced unity-gain bandwidth and DC gain and large slew rate with the same power consumption as the folded-cascode amplifier. Circuit level analysis and simulation results are provided to verify the effectiveness of the proposed amplifier.

Introduction: The folded-cascode amplifier (FCA) is usually utilised in low-voltage applications either as a single-stage or as the first stage in multistage amplifiers since it achieves high DC gain and relatively large signal swing. Moreover, the pMOS input pair is preferred over the nMOS one owing to its lower flicker noise, higher non-dominant pole, and lower input common-mode voltage [1]. Nonetheless, as shown in Fig. 1, to achieve a symmetric slewing behaviour, the equal bias current is employed in input and cascode transistors. As a result, the transistors M3 and M4 draw the most current acting only as current sources. Several techniques have been proposed to enhance the performance of FCAs such as the multipath schemes [2, 3] and the recycling folded-cascode amplifier [4]. In [2], the output current source active loads, M7-M10, are changed into active current mirrors. A complementary folded-cascode comprising of two input pairs is presented in [3] to exploit both nMOS and pMOS cascode transistors in the signal path. Moreover, in [3], a three-path amplifier comprising one folded-cascode, one current-mirror, and one current-mirror folded-cascode amplifier is presented. In [4], the transistors M1-M4 are split and the added input pair drives M3 and M4 through diode-connected transistors to make a two-path amplifier comprising one folded-cascode and one current-mirror amplifier. However, in all of these techniques, the current of one of the pMOS or the nMOS current source transistors is fixed and hence a small slew rate is achieved. In this Letter, a new class AB three-path single-stage amplifier is presented which considerably improves both large signal and small signal performance of the conventional FCA.

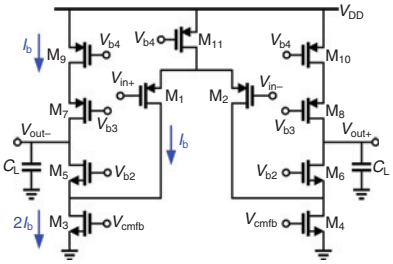

Fig. 1 *Conventional folded-cascode amplifier*

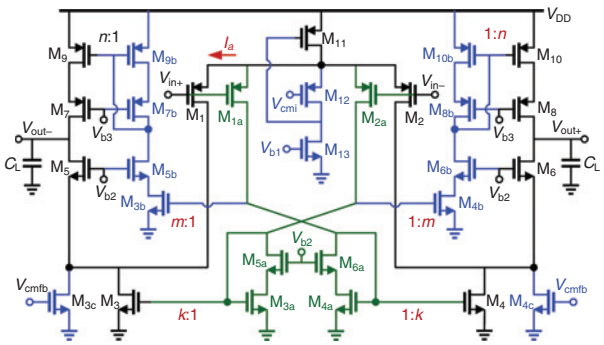

Fig. 2 *Proposed single-stage class AB amplifier*

Proposed amplifier: Fig. 2 shows the proposed amplifier. The transistors M1-M11 realise the conventional FCA. The input and nMOS current source transistors are split as M1, M1a, M2, M2a and M3, M3a, M4, M4a to make a two path amplifier as in [4]. M5a and M6a are used to form wide-swing cascode current mirrors for improved matching. Another path is employed to drive the gate of M9 and M10 to change them also as driving transistors. This is realised by wide-swing cascode current mirrors composed of M3b-M10b. A flipped voltage follower (FVF) cell comprising transistors M11-M13 [5] is employed to build the class AB operation in both input and cascode transistors. Transistors M3c and M4c are used to control the output common-mode voltage. V_{cmi} and V_{cmfb} denote the input common-mode voltage of the amplifier and the output control voltage of the common-mode feedback circuit, respectively. In reality, the proposed amplifier is built by the combination of three different amplifiers: a folded-cascode amplifier and two different current-mirror amplifiers.

Because of the class AB operation in the proposed amplifier, a large slew rate is achieved that is independent of the bias current. If, for instance, were V_{in+} to be much greater than V_{in-}, M1 and M1a enter the cutoff region and the drain current of M2a is increased by a large factor depending on the input step height. This is achieved because the source voltage of input transistors is fixed by the FVF cell since the drain current of M12 is constant and during slewing the gate-source voltage of input transistors is changed depending on their gate voltage variation. Hence, transistors M4a, M4, M3b, M9b, M9 turn off, while the drain current of M3a, M3, M4b, M10b, M10 is increased. On the other hand, since M4 turns off, the drain voltage of M2 is increased, making M6 to turn off. Thus, the load capacitor at positive output is charged by M10 and the load capacitor at negative output is discharged by M3. Therefore, we have:

$$SR^+ = \frac{mnI_{D2a}}{C_L}, \quad SR^- = \frac{kI_{D2a} + I_{D3c}}{C_L} \tag{1}$$

where I_{D2a} is the drain current of M2a during slewing, and k, m and n are the current mirror ratios as defined in Fig. 2. Usually $I_{D2a} >> I_{D3c}$, so to achieve a symmetric slewing behaviour we need to select $mn = k$. Thus the differential slew rate is given by:

$$SR \simeq \frac{2kI_{D2a}}{C_L} \tag{2}$$

During negative slewing a similar improvement in the value of slew rate is also obtained.

The DC gain and unity-gain bandwidth of the proposed amplifier are, respectively, given by:

$$A_{dc} = (g_{m1} + kg_{m2a} + mng_{m1a})R_{\text{out}} = (1 + k + mn)g_{m1}R_{\text{out}} \tag{3}$$

$$\omega_1 \simeq \frac{(g_{m1} + kg_{m2a} + mng_{m1a})}{C_L} = \frac{(1 + k + mn)g_{m1}}{C_L} \tag{4}$$

The total bias current of the proposed amplifier is as follows:

$$I_{total} = 4I_a + I_{D12} + 2mI_a + 2mnI_a \simeq (4 + 2m + 2mn)I_a \tag{5}$$

The same aspect ratio in input transistors of the proposed amplifier and the conventional FCA is considered to have equal input parasitic capacitors and hence the same feedback factor in the closed-loop configuration. Therefore, with equal power consumption, the transconductance of their input transistors is related by:

$$g_{m1} = \sqrt{\frac{1}{2 + m + mn}}\, g_{m1,fc} \tag{6}$$

where $g_{m1,fc}$ is the transconductance of input transistors in the conventional FCA. Hence, the unity-gain bandwidth and DC gain of the proposed amplifier is enhanced as:

$$A_{dc} = A_{dc,fc}\frac{(1 + k + mn)}{\sqrt{2 + m + mn}}\frac{R_{out}}{R_{out,fc}} \tag{7}$$

$$\omega_t = \omega_{t,fc}\frac{(1 + k + mn)}{\sqrt{2 + m + mn}} \tag{8}$$

Nonetheless, the phase margin of the proposed amplifier is degraded compared to the FCA since it has more non-dominant poles owing to the active current mirrors. For high-speed applications, it is necessary to move the non-dominant poles to higher frequencies. This can be achieved by choosing small current mirror ratios. For example, by considering $m = 1$, $n = k = 2$, both the DC gain and the unity-gain bandwidth of the proposed amplifier is enhanced about $\sqrt{5}$ times compared to the conventional FCA. The DC gain improvement will be more than $\sqrt{5}$ times since the output resistance in the proposed amplifier is also increased owing to using lower bias current in the output transistors.

Simulation results: To prove the effectiveness of the proposed amplifier, HSPICE simulation results were obtained using a 0.18 μm BSIM3v3 level 49 mixed-signal CMOS technology. The amplifier was designed for a switched-capacitor (SC) integrator with sampling and integrating capacitors of 5 and 10pF, respectively. The load capacitor was 5 and 1.7pF in AC open loop and transient closed loop simulations, respectively, which corresponds to an effective load capacitance of 5pF in both simulations. The conventional FCA shown in Fig. 1 was also simulated with the same power consumption and equal overdrive voltage in all signal path transistors except the input transistors (where the same aspect ratios were employed) in order to provide a fair comparison. Moreover, the minimum channel length was employed for high speed.

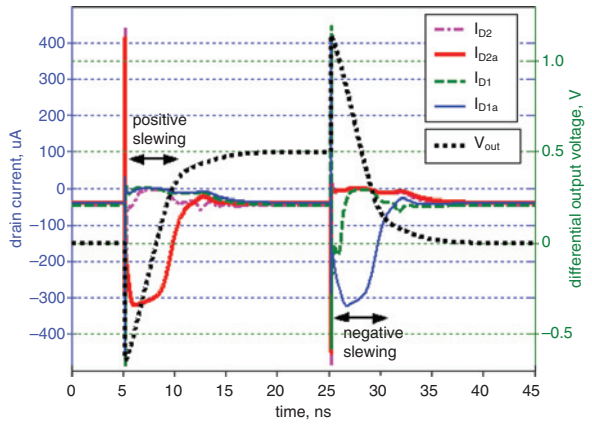

Fig. 3 *Open-loop frequency response of conventional folded-cascode and proposed amplifiers*

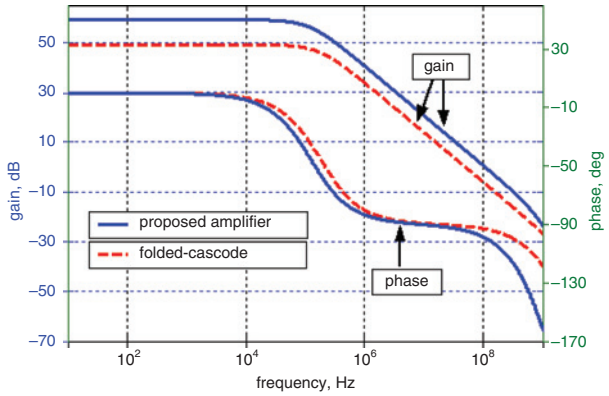

Fig. 4 *Simulated transient response*

The simulated open loop frequency and large signal transient responses are illustrated in Figs. 3 and 4, respectively. In large-signal transient simulations, an input step of 1V differential height was employed. Table 1 summarises the simulated results. The proposed amplifier achieves about 10.0 dB higher DC gain, 2.15 times larger unity-gain bandwidth and about 6.5 times larger slew rate than the conventional FCA, as theoretically expected. The large slew rate and enhanced unity-gain bandwidth of the proposed amplifier makes it to settle more rapidly than the conventional FCA in SC circuits. The input-referred noise voltage of both amplifiers is approximately the same. The active area of the proposed amplifier is larger than the conventional FCA. But, this is not a critical issue since the active area in mixed-signal circuits is mostly determined by passive components such as capacitors.

Table 1: Simulation results summary

Parameter	Folded-cascode	Proposed amplifier
DC gain	49.2 dB	59.2 dB
Unity-gain bandwidth	51.9 MHz	111.5 MHz
Phase margin (degree)	88.7	80.8
Average slew rate (V/μs)	36	233
0.01% settling time (t_{s+}/t_{s-})	65.8ns/63.9ns	22.1ns/21.8ns
Input-referred noise density at 100 kHz	115.7 nV/√Hz −138.7dBV_{rms}/vHz	125 nV/√Hz −138.1 dBV_{rms}/vHz
Static power dissipation (including bias circuitry)	663 μW	660 μW
Power supply voltage	1.5 V	
Technology	0.18 μm 1P6M CMOS	

Conclusions: A new single-stage class AB three-path operational amplifier is proposed. It achieves large slew rate and enhanced DC gain and unity-gain bandwidth by changing both nMOS and pMOS current sources in the conventional FCA as driving transistors and using a FVF cell to make the class AB operation. It can be used in high-resolution and fast-settling SC circuits where driving large capacitive loads is required.

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One or more of the Figures in this Letter are available in colour online.

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