A Free But Efficient Low-Voltage Class-AB Two-Stage Operational Amplifier

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***Abstract*—A simple and efficient low-voltage two-stage operational amplifier with Class-AB output stage is introduced. It has a large effective output current boosting factor (∼50) and close to a factor 2 bandwidth enhancement. This is achieved at the expense of minimum increase in circuit complexity and no additional static power dissipation. Experimental verification of the characteristics of the proposed circuit is provided.**

***Index Terms*—Analog integrated circuits, Class-AB amplifiers, low-voltage analog circuits, operational amplifiers.**

I. Introduction

TWO-STAGE or Miller op-amps [Fig. 1(a)] are the natural choice for low-voltage applications with resistive loads that require rail-to-rail output swing. For high slew rate requirements, a Class-AB output stage is commonly used in order to maintain low static power dissipation and with capability to generate output currents that are essentially larger than the output stage quiescent current $I^Q_{\rm OUT}$ [1]–[6]. Most Class-AB output stages can be considered implementations of the basic scheme shown in Fig. 1(b) where a floating battery with value $V_{\rm bat}$ is connected between the gate terminals of the output transistors operating as common source amplifiers. This causes output voltage variations at node X to be transferred to node Y and leads to Class-AB operation. A very important practical aspect is the incorporation of a circuit to control $I^Q_{\rm OUT}$. This circuit is used to adapt the value of $V_{\rm bat}$ so that the output current maintains the desired nominal value $I^Q_{\rm OUT} = I_{\rm D6Q} = I_{\rm D7Q} = I_b$ that remains independent of supply voltage and temperature variations, and technology parameters. Another important aspect in modern CMOS technology is the low supply and low power requirements for the Class-AB output stage and for the $I^Q_{\rm OUT}$ control circuitry. This due to the fact that, in order to prevent gate oxide breakdown, supply voltages in modern deep submicrometer CMOS technology have essentially reduced values (∼1.5 V) while transistor threshold voltages have remained relatively large (∼0.4 V). This has led to decreased headroom for $V_{\rm GS}$ variations and for the number of transistors that can be stacked between the supply rails. The difference between $V_{\rm DD}$ and the minimum supply requirements of the output stage $V_{\rm DD\,min}$ usually determines the maximum drain–source voltage of the output transistors $V_{\rm DS\,max}$ and with this the maximum output current and slew rate enhancement factor $I_{\rm o\,max}/I^Q_{\rm OUT} = (V_{\rm DS\,max}/V_{\rm DSQ})^2$ (where $V_{\rm DSQ}$ is the quiescent drain–source voltage of $M_{6,7}$).

Some common Class-AB schemes require a value $V_{\rm DD\,min}$ greater than two gate–source voltage (for example see [1]) and leave very small $V_{\rm DD}$ headroom for output current enhancement in modern CMOS technology with low supply voltage. Another important aspect for Class-AB circuits is that the additional current $I_{\rm Qcontrol}$ required by the quiescent current control circuitry adds to the static current consumption of the op-amp. This reduces the effective output current enhancement factor defined here by $\rm EOCEF = I_{o\,max}/(2I_b + I_{Qcontrol})$. This factor has a value $\rm EOCEF = 0.5$ for a Class-A op-amp with $I_{\rm o\,max} = I_b$. Assume for example, a circuit in a low supply voltage environment with $V_{\rm DS\,max} = 3V_{\rm DSQ}$ so that $I_{\rm o\,max} = 9I^Q_{\rm OUT}$ and a circuit (like that of [1]) with $I_{\rm Qcontrol} = 4I_b$. In this case, $\rm EOCEF = 1.5$. In spite of the fact that the maximum output current is relatively large in relation to I_b this corresponds to a modest EOCEF value due to the additional current and Silicon area required by the quiescent current control circuitry. In this paper we report a two-stage op-amp with a very compact hardware implementation of a Class-AB output stage and with $I_{\rm Qcontrol} = 0$. The proposed circuit has essentially the same static current requirements as the Class-A op-amp of Fig. 1(a) and the output stage has also the same minimum supply requirements: $V_{\rm DD\,min} = V_{\rm SD5} + V_{\rm SD2} + V_{\rm GS6}$. This value is close to a transistor's threshold voltage. An additional advantage of the proposed op-amp is that it shows enhanced phase margin and higher unity gain frequency than the conventional Class-A op-amp. Due to the fact that Class-AB operation and enhanced bandwidth is achieved with minimum additional hardware requirements and no additional static power dissipation or increased supply requirements (as opposed to other Class-AB op-amps currently in use) we denote the proposed architecture "free Class-AB op-amp." Experimental results of a fabricated test chip in 0.5-μm CMOS technology are shown that verify the characteristics of the proposed structure.

II. Proposed Circuit

Fig. 1(c) shows the proposed Class-AB op-amp. The only difference with respect to the conventional Class-A two-stage

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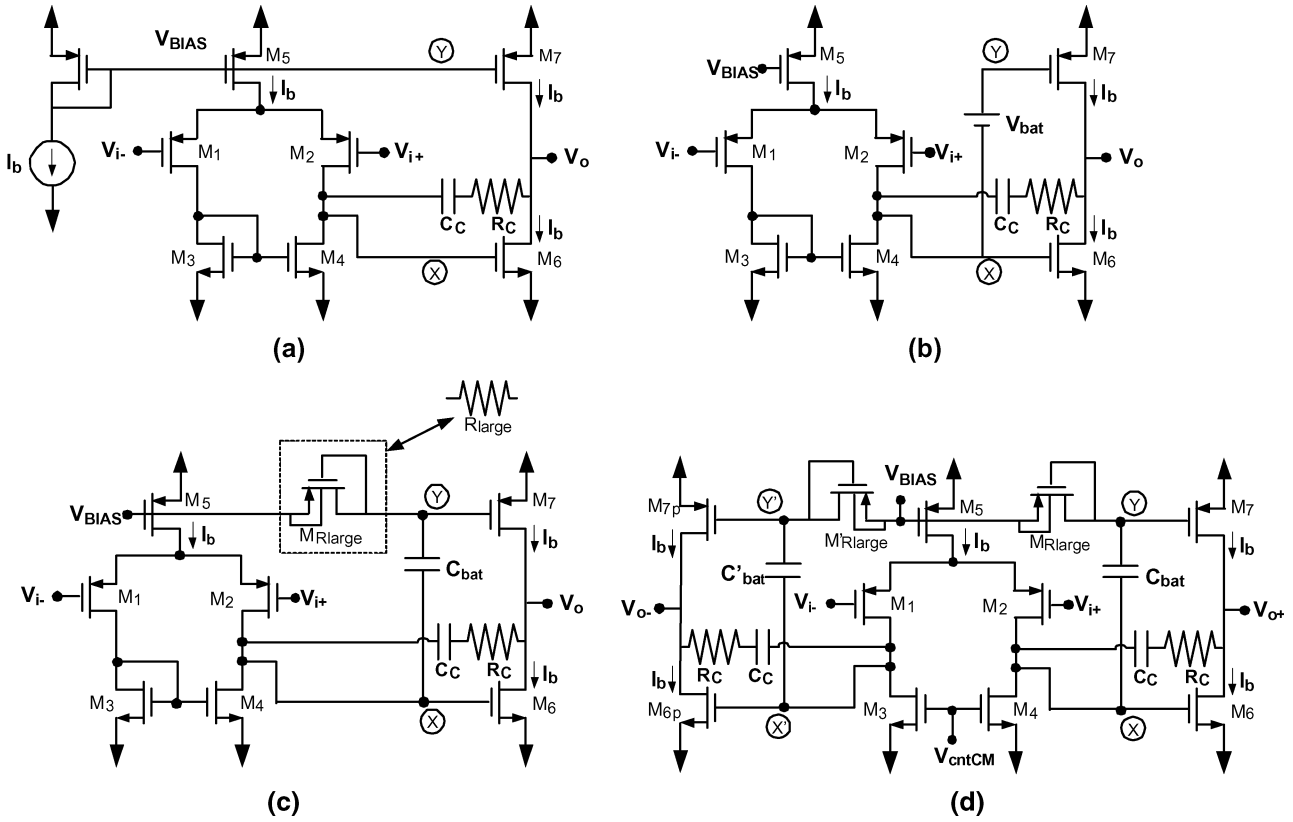

Fig. 1. (a) Conventional Class-A two-stage op-amp. (b) Conceptual scheme of two-stage op-amp with Class-AB output stage using floating battery. (c) Implementation of Class-AB output stage using large resistive element and capacitor. (d) Fully differential Class-AB op-amp.

op-amp of Fig. 1(a) is that the output stage includes a large resistive element implemented using a minimum size diode connected pMOS transistor $M_{R\text{large}}$ and a small valued capacitor C_{bat} Under quiescent conditions and given that no dc current flows through $M_{R\text{large}}$ the voltage at the gate of $M7$ is the same as at the gate of $M5$ so that the quiescent current in M5 and $M7$ has the same value I_b. Transistor $M6$ is commonly sized with W/L dimensions twice as large as those of $M3, M4$ so that the quiescent current in $M6$ has also a value I_b. During dynamic operation, when the output of the op-amp is slewing, the voltage at node X is subject to a large change. Given that capacitor C_{bat} can not discharge/charge rapidly through $M_{R\text{large}}$ it acts as a floating battery and transfers the voltage variations at node X to node Y. This provides Class-AB (push–pull) operation to the output stage.

A. Remarks

1) The value of C_{bat} can be small. Its minimum value is determined by the parasitic capacitance C_y at node Y(mainly the gate–source capacitance of $M7$) which forms a voltage divider with C_{bat}. This divider leads to attenuated voltage variations at node Y according to $V_Y = V_X C_{\text{bat}}/(C_{\text{bat}} + C_Y)$. A value of $C_{\text{bat}} > 2C_Y$ allows to transfer voltage variations from node X to node Y with relatively small attenuation. C_{bat} can be implemented using the gate–source capacitance of an MOS transistor operating in triode mode or with poly I poly II capacitors if available.
2) Transistor $M_{R\text{large}}$ is intended to operate as a very large resistive element (R_{large}). It is implemented by using a minimum size diode connected pMOS transistor with source and substrate terminal interconnected. It can also be implemented using a transistor biased in subthreshold according to the biasing techniques described in [7]–[9]. It operates in cutoff so that its on resistance is extremely high and corresponds to the leakage resistance of the N-well-source PN junction (this assuming N-well technology). A similar approach was proposed in [13], for narrowband applications. If larger bands are required, the authors propose the use of big capacitors or resistive elements placed out of chip or implemented with transistors in triode. The implementation proposed in this paper leads to a very wide band implementation starting at very low frequencies (on the order of 1Hz or lower), without the need of external elements or significant silicon area. It also features an increase of the gain-bandwidth product that also was not mentioned in [13].
3) Straightforward small-signal analysis of the circuit of Fig. 1(c) (with the capacitor C_{bat} replaced by a short circuit and $M_{R\text{large}}$ by an open circuit) shows that both, the proposed Class-AB op-amp and the conventional Class-A op-amp have the same gain-bandwidth products $\text{GB} = g_{m1,2}/C_c$ while the high frequency output pole shifts from a value $\omega_{\text{p2}} = g_{m6}/C_L$ for the conventional op-amp [10] to a value $\omega'_{\text{p2}} = (g_{m6} + g_{m7})/C_L$ for the proposed op-amp. This is due to the fact that both output transistors ($M6$ and $M7$) are active in the Class-AB output stage. This leads to a pole ω'_{p2} approximately a factor 2 larger: $\omega'_{\text{p2}} \approx 2\omega_{\text{p2}}$. Since ω_{p2} limits the maximum unity

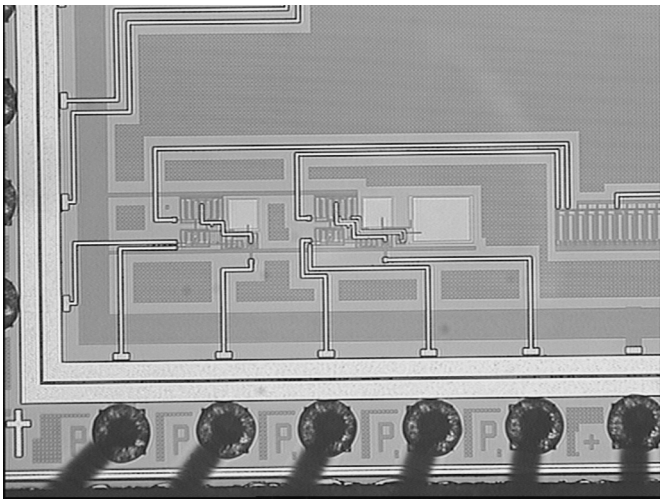

Fig. 2. Microphotograph of fabricated chip.

gain frequency the op-amp of Fig. 1(c) can be designed for a higher GB than that of Fig. 1(a). For equal GB values the op-amp of Fig. 1(c) has higher phase margin than that of Fig. 1(a). This is verified in the section on experimental results.

4) The output stage has low supply requirements since it can operate with a supply voltage close to a transistor's threshold voltage: $V_{\mathrm{DD\,min}} = V_{\mathrm{GS6}} + V_{\mathrm{SDsat2}} + V_{\mathrm{SDsat5}}$.
5) Due to Class-AB operation the proposed op-amp has approximately symmetrical slew rate. This as opposed to the conventional class-A op-amp that has commonly nonsymmetrical slew rate: a large negative slew rate determined by the large negative output current that can be delivered by $M6$ and a positive slew rate with value $\mathrm{SR} = I_b/(\mathrm{Cc}{+}C_L)$ limited by the constant current I_b in M7. Class-A op-amps can have symmetrical slew rate in cases where slew rate of the internal node X limits the slew rate of the op-amp [10].
6) In some cases the slew rate of Class-AB op-amps might be limited by the maximum current that the first stage can deliver to C_c in the internal node X. In this case a low voltage Class-AB differential input stage as that reported in [11], [12] can be used in order to achieve high slew rate at both the internal node and the output node of the op-amp.
7) The circuit shown in Fig. 1(d) is a fully differential version of the circuit of Fig. 1(b). It features similar characteristics as the single ended version but, as it is expected from a fully differential circuit, it has higher power supply and common mode rejection ratios than the single ended version.

III. Experimental Results

A test chip prototype including the circuits of Fig. 1(a) and (c) was fabricated in 0.5-μm CMOS (AMI-MOSIS) technology with nMOS and pMOS threshold voltages of about $V_{\mathrm{TN}} = 0.67$ V and $V_{\mathrm{TP}} = -0.96$ V, respectively. The following transistor sizes (in micrometers) were used: $M1, M2 : 30/1, M5, M7 : 60/1, M3, M4 : 10/1, M6 : 20/1$. $M_{R\mathrm{large}} : 2/1$, $C_{\mathrm{bat}} = 3$ pF, $C_c = 1$ pF, $R_c = 10\,\mathrm{k}\Omega$. Fig. 2 shows the microphotograph of the fabricated chip. The area of the Class-AB op-amp is $195 \times 63\ \mu\mathrm{m}^2$. The circuits

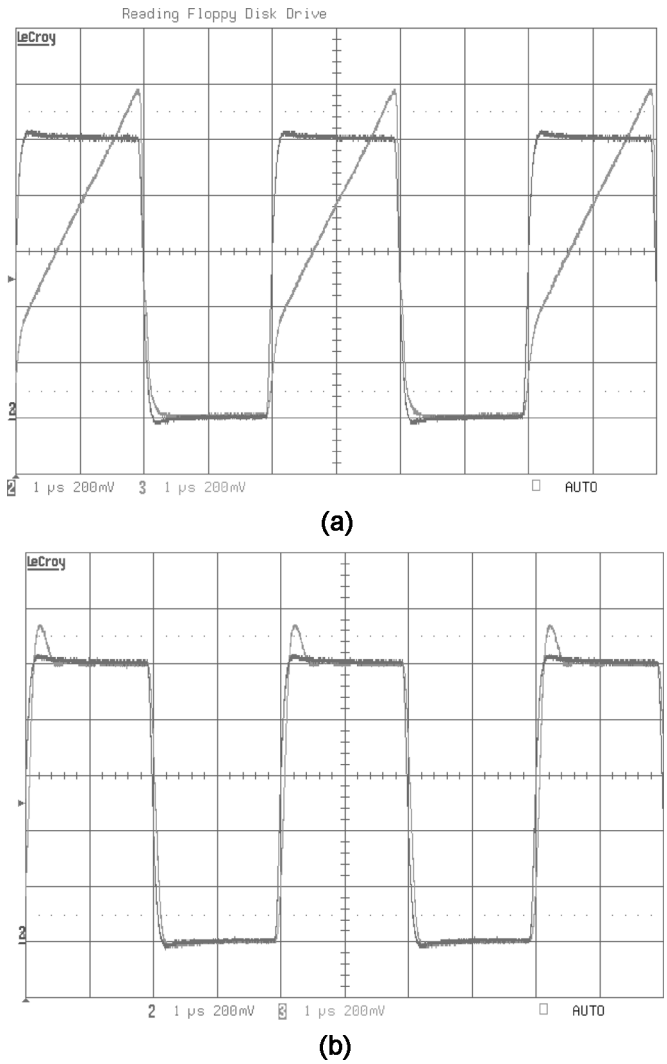

Fig. 3. Experimental pulse response input and output waveforms. (a) Conventional Class-A op-amp. (b) Free Class-AB op-amp of fabricated chip.

were tested with a single supply $V_{\mathrm{DD}} = 2$ V a bias current $I_b = 10\ \mu$A and $C_L = 25$ pF. Fig. 3(a) and (b) shows the experimental input and output waveforms of the op-amps of Fig. 1(a) and (c), respectively, for a 250-kHz 1-$\mathrm{V_{pp}}$ input square waveform. The corresponding measured slew rates were 0.410 and 20 V/μs. This corresponds to an effective slew rate enhancement factor of approximately 50. The large overshoot in the response of the Class-A op-amp is an indication of its reduced phase margin with respect to the Class-AB op-amp. Fig. 4(a) and (b) shows the measured ac open-loop response of the circuits of Fig.1(a) and (c). The measured unity gain frequencies are 6 and 11 MHz, respectively. The lower unity gain frequency for the Class-A op-amp is due the lower value of its output pole f_{p2}. Both op-amps can be seen to have the same $\mathrm{GB} = 11$ MHz. The measured open-loop dc gain was 45 dB in both cases. Measured values were in excellent agreement with simulations (not shown for the sake of space).

IV. Conclusion

A very simple implementation of a Class-AB two-stage op-amp was introduced. It has essentially the same static power

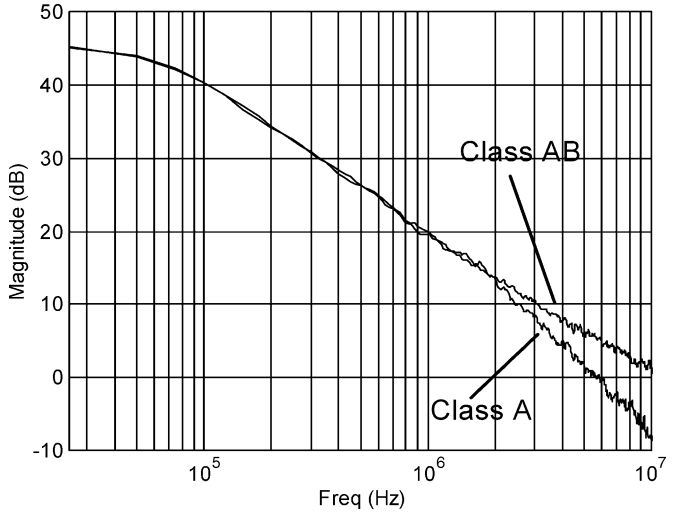

Fig. 4. Experimental open-loop responses of Class-A and Class-AB op-amps.

dissipation and circuit complexity of the conventional Class-A op-amp. As opposed to most previously reported Class-AB two-stage op-amps the proposed circuit is characterized by a large effective output current enhancement factor. It also features enhanced bandwidth greater phase margin and low supply requirements. The characteristics of the proposed circuit have been verified experimentally.

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