A –80dB HD3 Opamp in 3.3V CMOS Technology using Tail Current Compensation

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ABSTRACT

The proposed unity gain configuration operational amplifier (opamp) uses a new tail current compensation method to linearize the input differential pair. The circuit, fabricated in a 0.35um CMOS process, has HD3 less than -80dB up to 10MHz, and less than -60dB up to 80MHz input frequency. The supply voltage is 3.3V and signal amplitude is 1Vp-p. The opamp is well suited as a track and hold buffer.

1. INTRODUCTION

Track and Hold Amplifiers (THA) preceding broadband analog to digital converters for communication applications, have strong demand on linearity. In our solution for the THA it is necessary to buffer the input signal prior to the hold circuit. To implement this buffer a unity gain opamp is used.

The output stage is the main source of non-linearity in opamp circuits with current feedback and high or moderate loop gain. This is due to the high voltage swing on the output node. Opamp circuits with voltage feedback have a large voltage swing (Common Mode (CM) voltage) at the input nodes in addition to the output node. The proposed opamp is designed for unity gain configuration. Thus, the CM voltage is approximately equal to the input voltage. In this case the differential input stage is a considerable source of non-linearity [1].

Opamps designed for low frequencies achieves low distortion by applying high loop gain. The cause of this is that the feedback will suppress the harmonics caused by the differential input voltage [2]. At high frequencies there is a limit for the maximum loop gain. This limit is set by the fabrication technology. Then it is necessary to look at the sources of non-linearity and try to minimize the effects from these.

This paper takes a closer look on the differential pair and its contribution to non-linearity. In section 2 the differential pair is described. Assuming strong inversion, and thus high supply voltage (e.g. 5V), the variation in the transconductance gm as a function of the CM voltage is discussed in section 2.1. It is also described how this variation could be minimized [3], [4]. In section 2.2 the assumption is that the differential pair is operated in weak or moderate inversion which has to be the case for unity gain opamps at 3.3V supply voltage. The theory presented in section 2.2 is the foundation for the proposed opamp described in section 3. The goal for this new opamp circuit is low distortion at low supply voltage (3.3V) and high frequency, using a tail current compensation circuit.

Measurement of non-linearity at low levels is not straightforward, especially when the circuits are designed for on-chip applications. Section 4 describes the measurement system, and presents the measured results. Finally, the paper is summarized in section 5.

2. THE ORDINARY DIFFERENTIAL INPUT STAGE

2.1 Assumption: Strong inversion

An ordinary differential stage is shown in figure 1. M1 and M2 make the differential pair, and M3 supplies the tail current. The following assumptions are made: the transistors are in saturation, a simple square-law model, modified for channel length modulation, for the drain current applies (eq. (1)). V_S is approximately V_{CM} only shifted by V_{GS1}, V_D is constant and M3 has λ=0 (ideal current source). The transconductance gm could be expressed as eq. (2) and inserting eq. (3) for $V_{GS} - V_T$ leads to eq. (4). Eq. (4) shows that gm will decrease for an increase in V_{CM}, which means an increase in V_S. In [3] and [4] this is compensated for by making the gate length of M3 equal to the gate length of M1 and M2. Then the lambdas for these transistors are equal. Now, the tail current will increase with increasing CM voltage and could be expressed as eq. (5). Thus, gm remains approximately constant, as eq. (6) show. The drawback of this compensation method is that it is based on the square-law model of the MOS transistor, which is not valid when the transistors are in weak inversion.

$$I_{D1} = I_{D2} = \frac{1}{2}I_S = \frac{1}{2}\beta_1(V_{GS1} - V_{T1})^2(1 + \lambda_1 V_{DS1}), \quad V_{GS1} > V_{T1},\ V_{DS1} > V_{GS1} - V_{T1} \tag{1}$$

$$g_{m,s} = g_{m1,s} = g_{m2,s} = \frac{2I_{D1}}{V_{GS1} - V_{T1}} = \frac{I_S}{V_{GS1} - V_{T1}} \tag{2}$$

$$V_{GS1} - V_{T1} = \sqrt{\frac{I_S}{\beta_1(1 + \lambda_1 V_{DS1})}} \tag{3}$$

$$V_D \approx V_{D1} \approx V_{D2} \approx \text{constant},\quad V_{DS1} = V_D - V_S$$

$$\Rightarrow \quad g_{m,s} = \sqrt{I_S}\sqrt{\beta_1(1 + \lambda_1 V_D - \lambda_1 V_S)}, \tag{4}$$

$$I_S = I_{D3} = \frac{1}{2}\beta_3(V_B - V_{T3})^2(1 + \lambda_3 V_S) = \beta_3(1 + \lambda_3 V_S) \tag{5}$$

$$\Rightarrow g_{m,s} = \sqrt{\beta_3\beta_1}\cdot\sqrt{(1 + \lambda_1 V_D - \lambda_1 V_S)(1 + \lambda_3 V_S)}$$

$$= \sqrt{\beta_3\beta_1}\cdot\sqrt{1 + \lambda_1 V_D + (\lambda_3 - \lambda_1)V_S + \lambda_1\lambda_3(V_D - V_S)V_S}$$

$$g_{m,s} \overset{\lambda=\lambda_1=\lambda_3}{=} \sqrt{\beta_3\beta_1}\cdot\sqrt{1 + \lambda V_D + \lambda^2(V_D - V_S)V_S} \tag{6}$$

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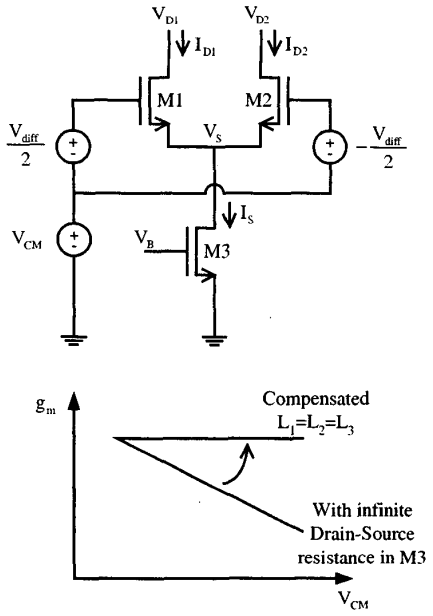

Figure 1. Compensation of tail current assuming strong inversion.

2.2 Assumption: Weak and moderate inversion

For low supply voltage, and low average CM voltage, M1 and M2 need to be designed for low V_{GS} voltage to keep M3 in saturation in the lower part of the input voltage range. $V_{GS} - V_T$ then approaches zero, and the transistors are on the edge of weak inversion, also called moderate inversion. Assuming weak inversion, eq. (7) could be used for the drain current, and eq. (8) for gm. Then, the compensation method mentioned above leads to an increase in gm, as shown in figure 2. In weak inversion gm/I_S is independent of $V_{GS} - V_T$. An increase in the CM level leads to an increase in the tail current and gm will increase. This could be compensated for by a current source with very large output resistance keeping I_S constant. This solution requires stacking of transistors, and is difficult because of the low supply voltage.

When operating the differential pair in moderate inversion the situation is more complicated than eq. (8) and (9) describe. Simulations show that improvement of the current source is not enough to keep gm constant. A decrease in tail current is necessary with increasing CM voltage to keep gm constant over the entire input voltage range.

For high frequencies the capacitor C_p in figure 2 reduce the impedance of the current source M3 even more. When the input voltage increases, and with that the CM voltage, C_p will be charged trough M1 and M2. As a result, gm will increase due to the increased drain currents. Opposite, when the input voltage decreases, the tail current I_S will discharge C_p, the drain current trough M1 and M2 decreases, and gm decreases.

$$I_S = 2I_{D1} = 2I_{D2} = 2n\beta V_{th}^2 e^{\frac{V_{GS1}-V_{T1}}{nV_{th}}}, V_{GS1} \le V_{T1}, \text{and saturation} \quad (7)$$

$$g_{m,w} = g_{m1,w} = g_{m2,w} = \frac{I_S}{2nV_{th}} \quad (8)$$

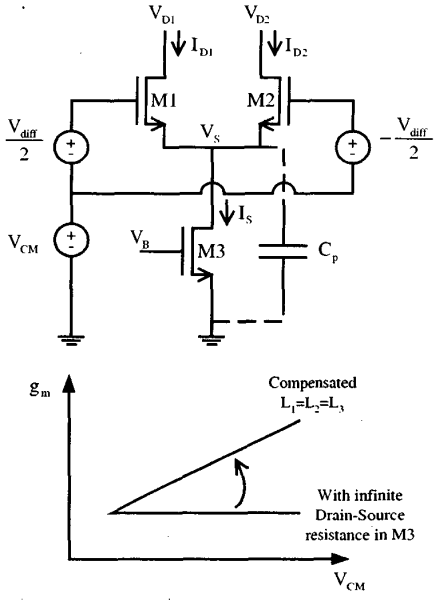

Figure 2. Compensation of tail current assuming weak inversion.

3. TAIL CURRENT COMPENSATION CIRCUIT

Using a tail current compensation circuit one could compensate for an increase in tail current, due to increasing CM-voltage. This circuit indirectly measures the tail current and subtracts the increase from the tail current of the differential pair. This is implemented in the proposed opamp, which is shown in Figure 3.

Transistors M1 to M14 make a one-stage opamp with a differential input pair and a folded cascode output stage. The tail current compensation circuit is constructed by M1b to M10b. M1b to M3b is a copy of M1 to M3 but scaled down by a factor 4 to save current. M6b is measuring the tail current of M1b and M2b, and thereby indirectly measuring the tail current of M1 and M2. By adjusting the current gain in M6b to M9b it is possible to subtract the right amount of current to compensate for the variations in tail current in M1 and M2 due to the input voltage. The optimization for minimum HD3 is done for high frequencies, and with the differential input stage and the folded cascode output stage together. HD2 will be suppressed by the differential circuit configuration used in THA, and is not important.

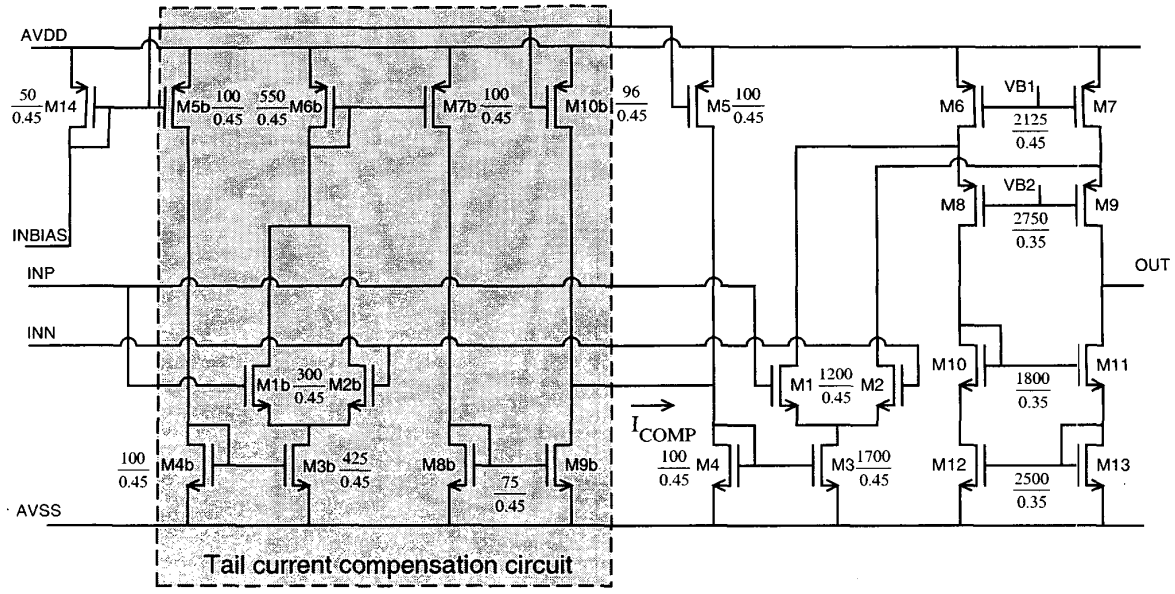

Figure 3. Opamp with tail current compensation circuit. The opamp is design for unity gain configuration optimized for low HD3.

4. MEASUREMENT SYSTEM

The measurements are carried out using the test setup described in figure 4. A band-pass filter is used to suppress the harmonics of the signal generator. Because of the suspected contribution to the non-linearity the protection diodes in the pads have been removed. Further, due to a large off-chip load, a voltage buffer supplied from a higher supply voltage is used. The higher supply voltage makes it easier to do a low distortion voltage buffer, which is a modified source follower. An on-chip capacitive voltage divider is used to lower the signal amplitude for the buffer with a factor D=0.45, and thus lower the harmonics generated by the buffer. The divider also makes the necessary shift in bias voltage. The output signal from the test-chip is applied to a resistive voltage divider to match the signal to the 50 Ohms load of the spectrum analyzer.

Measuring low levels of non-linearity are very difficult, especially when the Device Under Test (DUT) are designed for an on-chip load. This requires the use of a buffer to bring the signal off-chip. Ideally, the buffering element should not contribute to the non-linearity, but this is not possible when DUT is already on the edge of the technology. The on-chip buffer will contribute to the non-linearity measured at the output pin, which makes it necessary to estimate HD3 of the opamp.

The transfer function for the unity gain opamp and the voltage buffer could be expressed as eq. (9) and (10) respectively. The coefficients a_i and b_i are frequency dependent and are expressed in polar form by a magnitude ($|a_i|$ and $|b_i|$) and a phase (ϕ_{ai} and ϕ_{bi}). From the theory of Volterra series, as presented in [5], the output from the test-circuit is given by eq. (11). Here, "the test-circuit" means the unity gain opamp followed by the capacitive voltage divider and the voltage buffer.

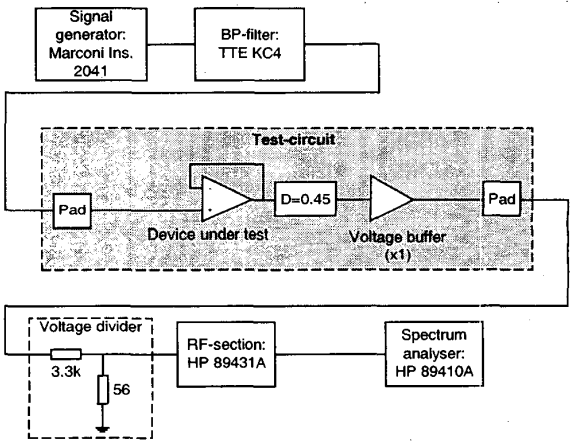

Figure 4. Measurement system.

To estimate HD3 of the opamp (HD3_O) the on-chip buffer is characterized alone, with the same bias and signal conditions as it is exposed to when buffering the opamp. From these results, and HD2_S and HD3_S of the opamp and buffer in series it is possible to estimate HD3_O as eq. (12) describe. Here, $\phi_{HD2,B}$ and $\phi_{HD3,B}$ are the phase of HD2_B and HD3_B respectively, $\phi_{HD2,S}$ and $\phi_{HD3,S}$ are the phase of HD2_S and HD3_S respectively, and $\phi_{HD2,O}$ is the estimated phase of HD2_O. In these measurements only the amplitude of the harmonics is considered. Thus, it is possible to estimate best and worst case curves for HD3_O (eq. (13) and (14) respectively).

$$V_{out,O} \approx |a_1| e^{j\phi_{a1}} V_{in,O} + |a_2| e^{j\phi_{a2}} V_{in,O}^2 + |a_3| e^{j\phi_{a3}} V_{in,O}^3 \quad (9)$$

$$V_{out,B} \approx |b_1| e^{j\phi_{b1}} V_{in,B} + |b_2| e^{j\phi_{b2}} V_{in,B}^2 + |b_3| e^{j\phi_{b3}} V_{in,B}^3 \quad (10)$$

$$\begin{aligned} V_{out,S} \approx & \left(D \cdot |a_1| \cdot |b_1| e^{j(\phi_{a1}+\phi_{b1})}\right) V_{in,O} \\ & + \left(D^2 \cdot |a_1|^2 \cdot |b_2| e^{j(2\phi_{a1}+\phi_{b2})} + D \cdot |b_1| \cdot |a_2| e^{j(\phi_{b1}+\phi_{a2})}\right) V_{in,O}^2 \\ & + \left(\begin{array}{l} D^3 \cdot |a_1|^3 \cdot |b_3| e^{j(3\phi_{a1}+\phi_{b3})} + D \cdot |b_1| \cdot |a_3| e^{j(\phi_{b1}+\phi_{a3})} \\ + 2D^2 \cdot |a_1| \cdot |a_2| \cdot |b_2| e^{j(\phi_{a1}+\phi_{a2}+\phi_{b2})} \end{array}\right) V_{in,O}^3 \end{aligned} \quad (11)$$

$$HD3_O \approx 20 \cdot \log\left(\left| 10^{\frac{HD3_S}{20}} \cdot e^{j\phi_{HD3,S}} - |a_1|^2 \cdot 10^{\frac{HD3_B}{20}} \cdot e^{j(\phi_{HD3,B}+2\phi_{a1})} \right.\right. \left.\left. - 2 \cdot |a_1| \cdot 10^{\frac{HD2_B+HD2_O}{20}} \cdot e^{j(\phi_{HD2,B}+\phi_{HD2,O}+\phi_{a1})} \right|\right) \quad (12)$$

$$HD3_{O\_B} \approx 20 \cdot \log\left(\left| 10^{\frac{HD3_S}{20}} - |a_1|^2 \cdot 10^{\frac{HD3_B}{20}} - 2 \cdot |a_1| \cdot 10^{\frac{HD2_B+HD2_O}{20}} \right|\right) \quad (13)$$

$$HD3_{O\_W} \approx 20 \cdot \log\left(\left| 10^{\frac{HD3_S}{20}} + |a_1|^2 \cdot 10^{\frac{HD3_B}{20}} + 2 \cdot |a_1| \cdot 10^{\frac{HD2_B+HD2_O}{20}} \right|\right) \quad (14)$$

The results are shown in figure 5. The bold curves (without dots) are the estimated values for the best case (lower) and worst case (upper) of HD3_O. The HD3_B curve is the measured third harmonic of the buffer, and HD3_S is from the combination of the opamp and buffer, with input amplitude at 1Vp-p. The worst case curve gives a third harmonic which is better than –80dBc for frequencies up to 10MHz and better than –60dBc for frequencies up to 80MHz.

The die photograph is shown in figure 6. The opamp followed by the capacitive voltage divider and the voltage buffer is shown in the upper left corner. The voltage buffer is placed in the lower right corner.

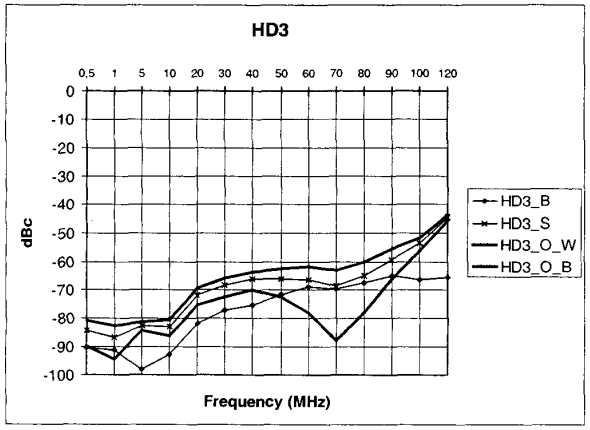

Figure 5. HD3 versus frequency for the output voltage buffer alone (HD3_B), the opamp followed by the buffer (HD3_S) and the estimated best case (HD3_B, the lower bold curve) and worst case (HD3_W, the higher bold curve) for the opamp. The input signal amplitude is 1Vp-p for the opamp. Note: Frequency axe is linear between 10 and 100 MHz only.

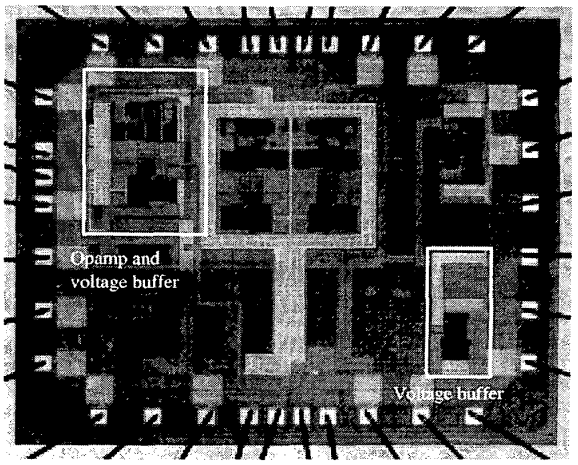

Figure 6. Die photograph. The opamp followed by the voltage buffer is in the upper left corner, and the voltage buffer alone is in the lower right corner. For estimation of HD3_O the voltage buffer was measured as a stand- alone device with the same bias and signal conditions as the voltage buffer following the opamp.

5. Summary

A broadband, low supply voltage, unity gain opamp using a tail current compensation circuit to achieve low distortion at high frequencies has been described in this paper. The tail current compensation circuit indirectly measures the variation of the tail current in the input differential pair, and compensates for it. The circuit has been optimized for low HD3 at high frequencies, and fabricated in a 0.35um CMOS process. Measurements showed that HD3 is less than -80dB up to 10MHz, and less than -60dB up to 80MHz input frequency. The supply voltage was 3.3V and the signal amplitude was 1Vp-p.

6. REFERENCES

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