A Review of Watt-Level CMOS RF Power Amplifiers

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***Abstract*—This paper reviews the design of watt-level integrated CMOS RF power amplifiers (PAs) and state-of-the-art results in the literature. To reach watt-level output power from a single-chip CMOS PA, two main strategies can be identified: use of high supply voltage and use of matching and power combination. High supply voltage limits are closely related to device design in the fabrication process. However, the maximum operating voltage can be improved by amplifier class selection, circuit solutions, and process modifications or mask changes. High output power can also be reached by the use of on-chip matching and power combination, commonly using on-chip transformers. Reliability often sets the limits for the PA design, and PA degradation mechanisms are reviewed. A compilation of state-of-the-art published results for linear and switched watt-level PAs, as well as a few fully integrated CMOS PAs, is presented and discussed.**

***Index Terms*—CMOS power amplifiers (PAs), integration, system-on-chip (SoC).**

I. Introduction

A. CMOS for Wireless System-on-Chip (SoC)

THE WIRELESS market has experienced a remarkable development and growth since the introduction of the first modern mobile phone systems, with a steady increase in the number of subscribers, new application areas, and higher data rates. Much of these advancements are due to successful high-level integration of the electronic circuitry in low-cost technologies. To continue this development, we need full integration of the RF, analog, and digital parts that constitutes a modern radio into SoC radios. Only modern CMOS technology has the potential to do this.

CMOS has for a long time been the choice for digital integrated circuits due to its high level of integration, low cost, and constant enhancements in performance. Due to the significant scaling of MOS transistors, the transition frequency has reached well beyond 100 GHz [1] and CMOS technology have become popular in RF applications.

During the last decade, considerable effort has been spent on researching Si- and CMOS-based RF integrated circuits (RFICs) for wireless handheld applications [2]–[5]. The digital baseband circuits have now successfully been integrated in CMOS, as well as most of the radio building blocks. To lower the cost and to achieve complete integration of a radio SoC, it is desirable to also integrate the power amplifier (PA) in a single CMOS chip [6]–[10]. Whereas digital circuits benefit from the technology scaling, it is becoming harder for the radio, and especially the PA, to meet requirements on linearity, output power, bandwidth, and efficiency using the low supply voltages that follow from technology scaling. However, the almost-for-free integration of CMOS opens up possibilities for new PA architectures.

For the PA, the path to the fully integrated SoC can be seen as a two-step process. The first step is the standalone integrated CMOS PA, using as few external components as possible, fabricated in the same technology as the SoC. The first watt-level fully integrated CMOS PA, with on-chip matching to 50 Ω, was published in 2001 [11] using a transformer power combination technique known as distributed active transformers (DATs), and linear PAs blocks. A literature survey of published CMOS PA results [9] shows reported output powers of about 33–34 dBm (2–2.5 W) at 1–2 GHz, about 20 dBm (0.1 W) at 5–6 GHz, and then dropping to below 20 dBm at higher frequency. Section V in this paper contains more detailed compilations of different architecture watt-level CMOS PAs, but the findings are similar.

The second step is to integrate the PA with the baseband/radio SoC and solve the problems caused by the integration. For communication standards with peak output power less than 30 dBm, complete SoCs are common in products today, such as wireless local area networks (WLANs) [12]–[14], shared Bluetooth and WLAN [15], as well as digitally enhanced cordless telecommunications (DECT) [16]. They include integrated PAs, however most of them are not delivering maximum allowed output power in accordance with the standards.

For cellular handsets, SoCs with full output power are virtually nonexistent. However, a third-generation (3G) RF transceiver with an integrated PA in 65 nm was recently presented by the Intel Corporation [17] although detailed specifications have not been released. Standalone second-generation (2G) handset integrated CMOS-PAs have been commercially available on the market for a number of years [18]–[21]. For 3G (WCDMA) PAs, the groundbreaking work has been done by startup companies, such as Amalfi Semiconductor (now acquired by RFMD), Black Sand Technologies [22], and Javelin Semiconductor (now acquired by Avago) [23], [24]. Standalone 3G PAs are now available on the market. The first CMOS PA capable of 4G (LTE) operation at all bands was recently presented [25].

Due to the low breakdown voltages for fast CMOS devices, other technologies, such as GaAs HBT [26], [27], Si bipolar [28], [29], SiGe HBT [30]–[32], and low-voltage LDMOS [33], [34] have thus far dominated the small-size PAs. See [35] for CMOS versus GaAs comparison for mobile phone PAs, and [36]

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for comparison of different bipolar technologies for similar applications.

Since the integration level generally is lower for such technologies, commercial PAs for mobile phones often appear in the form of modules where one or several dies are mounted on an organic or ceramic substrate that also contains the output-matching network [37]–[40]. Considering the low price and maturity of GaAs-based PA modules, the advantages of CMOS-based PA modules are not so clear.

Integration has its own drawbacks. The PA generates excessive heat, can cause crosstalk and disturbance on other chip parts, and occupies large (expensive) chip area because of the integrated passives necessary for matching and power combination.

Existing radio solutions may need to be redesigned to achieve the robustness that the PA integration requires [41]. Between the PA and the antenna, there is a need for additional components, such as additional matching, filters, circulators, and switches [42], [10]. These components may be put together in a separate front-end module (FEM), including the PA [25].

Thus far, we have mainly discussed PAs for mobile (battery operated) operation. On the infrastructure side, there is another potential large market. If the PAs can handle high (peak) output power and thus signals with high peak-to-average power ratio (PAPR), new markets for CMOS PAs will open, such as small (picocell and femtocell) basestation PAs. The newer WLAN standards (e.g., 801.11ac) also utilize high PAPR. This will require the PA to handle high (say, 34–40 dBm) peak power. As the average power is about the same level as a mobile phone PA (about 24 dBm, maybe up to 30 dBm), the actual power dissipation will be similar for many applications.

B. Strategies to Achieve Watt-Level CMOS PAs

For a mobile phone or WLAN PA to deliver >1 W peak output power at RF into a load is very demanding. The power P delivered from a PA with a sinusoidal signal, at a peak voltage amplitude V, into an ohmic load R can be described as

$$P = \frac{V^2}{2R}. \tag{1}$$

To deliver 1-W power into a 50-Ω load, we would need 20-V peak-to-peak voltage swing, which is much higher than the 1–2 V we could afford over a modern CMOS transistor. For a PA with maximum of 2-V peak-to-peak voltage swing and a 50-Ω load, the output power would only be about 10 mW (10 dBm). As the reduction of geometries and supply voltages continues, generating high output power in CMOS becomes more challenging.

Two main strategies to reach high output power can be identified from (1), which are: 1) increased supply voltage and 2) reduced load (trading current for voltage). Limits for high supply voltage come mainly from the device design in the fabrication process and the layout, but these can be partially worked around using circuit design-related improvements. For the load, we need to interface to 50 Ω, which means using different load transformation and power-combining structures.

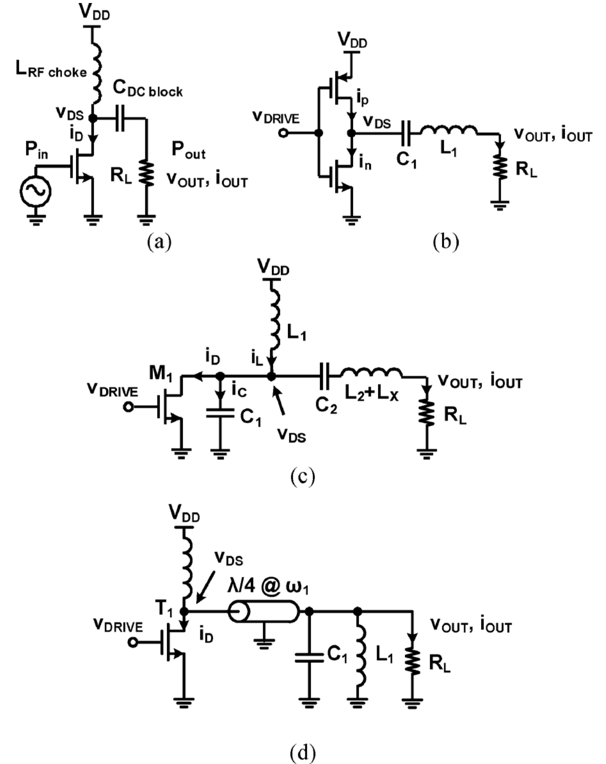

Fig. 1. Most important PA classes. (a) Class-A/B/C (linear). (b) Inverter-based class-D (switched). (c) Class-E (switched). (d) Class-F (switched).

C. Outline of Text

This paper reviews the background and state-of-the-art of an integrated CMOS-PA with the focus on high-power output, while keeping linearity and efficiency at a reasonable level. The performance of linear class-A/B, polar modulated, and outphasing PAs will be compared. To be more precise, we are interested in the limits of obtaining high output power (watt level) at telecommunication radio frequencies (about 0.5–6 GHz), using device technology mainly available via commercial CMOS foundry technology, to achieve PAs with high integration (single-chip PAs), suitable for SoC. The driving applications are WLAN and cellular, both terminal and infrastructure devices.

In Section II, we review different ways to increase the supply voltage using circuit-related workarounds and using improved device structures. In Section III, we review methods and limitations of load reduction by matching and power-combining PA architectures. In Section IV, we will discuss PA reliability concerns. In Section V, state-of-the-art CMOS PAs will be reviewed, and in Section VI, we draw conclusions and discuss the future of CMOS-PAs.

II. Strategy: Supply Voltage

A. Introduction

According to (1), output power increases as the square of the supply voltage. Operating the PA at as high supply voltage as possible is therefore desirable. However, modern nm-CMOS devices are limited with respect to maximum allowed supply voltage because of low device breakdown voltages (a couple of

TABLE I
COMPARISON OF THE PROPERTIES OF DIFFERENT PA CLASSES (MANY OF THE NUMBERS DERIVED FROM [46])

Class	Maximum drain efficiency [%]	Peak drain voltage	Peak drain current[a]	Maximum output power	Normalized power output capability[b]
A	50	$2*V_{dd}$	$2*V_{dd}/R$	$V_{dd}^2/(2R)$	0.125
B	78.5	$2*V_{dd}$	$2*V_{dd}/R$	$V_{dd}^2/(2R)$	0.125
C[c]	100[d]	$2*V_{dd}$	$2*V_{dd}/R$	$V_{dd}^2/(2R)$	0.125
inverter-based switched D	100	$1*V_{dd}$	V_{dd}/R	$\frac{\left(\frac{2}{\pi}V_{dd}\right)^2}{2R}$	0.32
switched E	100	$3.6*V_{dd}$	$1.7*V_{dd}/R$	$0.577*V_{dd}^2/R$	0.098
switched F	100	$8*V_{dd}/\pi \approx 2.5*V_{dd}$	$\frac{8}{\pi R}V_{dd}$	$\frac{\left(\frac{4}{\pi}V_{dd}\right)^2}{2R}$	0.16

[a] For the fundamental tone.
[b] Dimensionless ratio of actual output power to the product of the maximum device voltage and current, [46] p. 497.
[c] Maximum/peak values are not obtained for the same conduction angle φ.
[d] Approaches 100 % as the conduction angle φ goes to 0, but so does the output power as well.

volts) and reliability (gate oxide, hot electrons) concerns [43], [44]. As most PA classes generate peak voltage higher than the supply voltage (see Section II-B), junction breakdown voltages of two times, up to four times, the supply voltage may be needed. Additional margin may also be needed to achieve *robustness* during handling or mismatch conditions, which can create high voltage peaks at the PA output.

To stretch the limits of the maximum allowed supply voltages, there are several approaches, which are: 1) use PA classes that reduce the ratio of device breakdown voltage to supply voltage, as will be discussed in Section II-B; 2) use circuit solutions that can handle high supply voltage, Section II-C; and 3) use devices with high breakdown voltages, Section II-D.

B. PA Classes and Architectures for High Output Power

The voltage stress over the internal nodes of the PA is related to the PA class. It is assumed that the reader is familiar with the most common PA classes, otherwise see [45] for a general overview and [46] for a CMOS oriented overview. Simplified schematics of the most important classes are shown in Fig. 1, and in Table I a selection of amplifier properties for the most important classes is shown. There are also many variants of the basic classes, such as inverted class-E, inverted class-F, etc. [45], and classes beyond F, but these mostly lack common definitions, at least for use at RF, and will not be discussed further.

All linear PA classes A, B, and C use the same topology [see Fig. 1(a)], but different input bias (gate voltage) levels, which causes the PA to switch off part of the signal cycle. This will cause tradeoffs in output power, dc standby current, linearity, and efficiency.

The most popular class, the linear class-AB, is not listed in Table I; it is biased somewhere between class A and B and inherits most of the properties of these amplifiers. For simpler modulation signals, it has been a common choice for a long time as it offers a good tradeoff between linearity, efficiency, and standby current. The linear PAs will theoretically experience up to two times the supply voltage on their output transistor node during normal operation. For CMOS devices, the maximum allowed drain-to-substrate and drain-to-source voltages must therefore be at least two times the supply voltage. State-of-the-art watt-level linear integrated CMOS PAs will be discussed in Section V (Table II).

By operating the transistors as switches instead of current sources as in linear PAs, amplifiers can achieve theoretical efficiency up to 100%. The inverter-based switched class-D is shown in Fig. 1(b). Basically being an inverter, the class-D amplifier has a peak voltage that will not exceed the supply voltage. Other benefits of class-D PAs are load impedance insensitivity and high bandwidth. However, high-performance inverter-based class-D RF amplifiers require fast p-devices, which have not been available until about the 130-nm CMOS node. Integrated RF class-D PAs in CMOS have therefore only recently appeared in the literature (see Section IV, Table IV). The class-D PAs suffer from short-circuit power dissipation, power consumption due to drain capacitance switching, and power losses due to the strong harmonics. All these effects have recently been addressed [47], [48].

The switched class-E has been quite popular in large discrete PAs. It addresses the class-D loss mechanisms due to the parasitic capacitance of the output stage by shaping the drain voltage with reactive load impedance [seeFig. 1(c)] in order to decrease the drain voltage to zero as the switch turns on, to minimize the charges stored on the drain capacitance. The maximum theoretical peak voltage is about three and a half times the supply, which is a major drawback. Using a finite inductance instead of an RF-choke [L1 in Fig. 1(c)], the peak voltage can be reduced to two and a half times the supply [49], [50]. Higher output power, higher load resistance, or higher efficiency, can also be achieved using a finite inductance [50]. State-of-the-art watt-level switched class-E integrated CMOS PAs will be discussed in Section V (Table III).

The related class-F also employs drain voltage waveform shaping to achieve a high efficiency, but uses a $\lambda/4$ transmission line at the drain and a high-Q tank in parallel with the load resistor. The theoretical peak voltage is slightly above two times the supply, marginally higher than the linear classes. However, to achieve a high efficiency, several resonators with

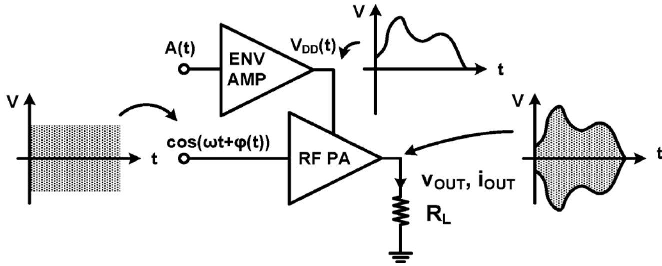

Fig. 2. Polar modulation.

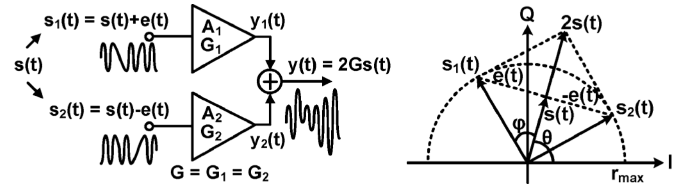

Fig. 3. Outphasing modulation.

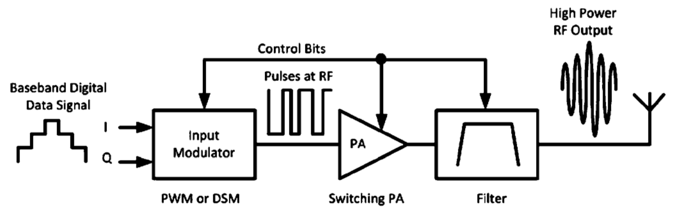

Fig. 4. PWM [57].

a high Q are needed, requiring additional area. The $\lambda/4$ transmission line also cannot be directly integrated.

One drawback with switched amplifiers is that there is no linear relationship in amplitude between the input signal and the output signal. Additional methods or architectures must therefore be used for amplitude modulation and linearization, which often requires additional blocks and/or redesign of the transmitter architecture, even including the baseband. The different methods can be divided into three groups: supply modulation using polar transmitters [51], [52], outphasing (Chireix [53] and LINC [54]), and pulsewidth modulation [55], [56].

The polar modulation (Fig. 2) combines a nonlinear RF PA with an envelope amplifier (ENV AMP) for supply voltage modulation to achieve a highly efficient linear PA (most commonly used with class-E PAs, where the drain efficiency does not depend on the supply voltage). The linearity of the amplitude modulator must be good and have a large bandwidth due to the bandwidth expansion of the envelope signal. It is also important to align the amplitude and phase paths (the RF path) in the polar transmitter to ensure a clean spectrum despite the bandwidth expansion of the two signals.

A few watt-level polar modulated PAs in CMOS have been demonstrated, mostly using class-E (see Section V, Table V), but none is a true single-chip integrated PA.

In the outphasing concept (Fig. 3), an amplitude- and phase-modulated signal, $s(t)$, is decomposed into two constant amplitude signals, $s_1(t)$ and $s_2(t)$, containing the original signal and the quadrature signal, $e(t)$. The two constant amplitude signals are separately amplified by two PAs and then recombined in a power combiner, where the quadrature signals cancel each other as long as the power combiner is linear and the two amplifier paths are well balanced. Common ways to realize the power combiner are using a matched combiner with isolation [58], which suffers from low efficiency unless the power is recycled [59], on-chip [60]–[62] or off-chip [63] $\lambda/4$ transmission lines, or connecting the load directly between the two amplifier outputs using a transformer [64].

The outphasing PAs suffers from bandwidth expansion, similar to the polar modulated PAs. To improve linearity and mitigate amplitude and phase mismatches between the signal branches, the supply voltages for the output stages (for amplitude mismatch) and the phases (for amplitude and phase mismatches) should be made adjustable [65].

Watt-level outphasing PAs in CMOS have only been demonstrated using switched class-D architectures (see Table IV). One reason may be that class-E PAs are less suitable for linear operation with nonisolating combiners as the constant envelope operation of the Class-E PA is ruined due to the varying load impedance.

Pulsewidth modulation (PWM) (Fig. 4) is becoming more popular for switched amplifiers. Traditionally used to modulate the input of class-D PAs (sometime referred to as class-S amplifier [45]), but now being used with all types of switched amplifiers [66], [67]. PWM PAs are mainly limited due to the minimum pulsewidth that the PA can process without pulse swallowing. We have not found any watt-level fully integrated PWM modulated PAs in the literature, but one polar modulated multichip is demonstrated in [68] (see Section V, Table V).

Most amplifiers can benefit from additional linearization to be able to fulfill requirements on parameters such as adjacent channel power ratio (ACPR) and error-vector magnitude (EVM), while still keeping the output power and efficiency high. Design methods to improve the linearity include additional circuitry to keep the input bias stable for different signal levels, or adjusting the characteristics of individual stages in a multi-stage amplifier. Such improvements are usually classified as analog predistortion (APD), and are mostly used with the linear PA-classes [69]. Linearity can also be improved by modifying the amplitude and phase of the baseband signal before the RF modulation, known as digital predistortion (DPD) [70]. This requires system-level design of both baseband and RF parts, which increases the complexity of the transmitter.

The maximum efficiency, as listed in Table I, only occurs for the linear classes at some optimum output power level, often close to the $\mathrm{P}-1$ dB point. At lower output power, the efficiency drops rapidly. Efficiency is also reduced in real amplifier implementation because of imperfections and losses in the active and passive components. This is especially true for the switched PA classes, although having high theoretical maximum efficiency (up to 100%), the actual numbers quickly drop, as evident from Tables III–V.

As modern high data rate signals use advanced modulation techniques where the peak amplitude is 10–12 dB higher than the average signal (PAPR) during transmission, the output power must be reduced, *backed-off*, typically with the PAPR

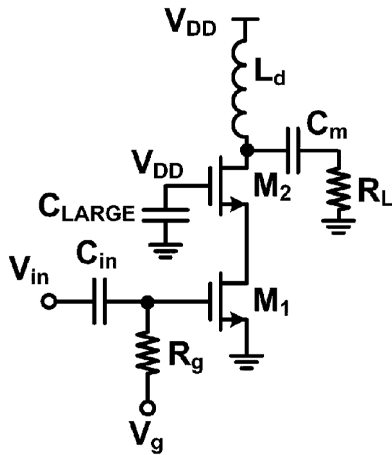

Fig. 5. Cascode.

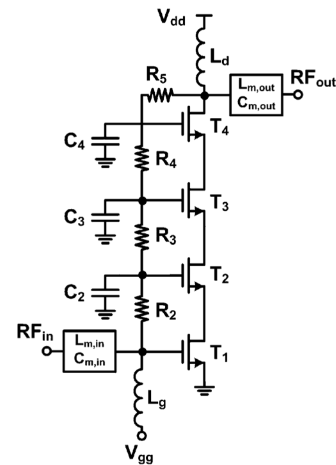

Fig. 6. HiVP configuration with four devices [81].

value to maintain linear amplification [71]. The average efficiency then drops drastically, maybe from more than 50% to only 5% at 10 dB back-off.

There are many methods to improve the efficiency in back-off [72], from simple bias point or supply voltage changes, to architectural level changes. The Doherty amplifier architecture is a very old example of improved efficiency during back-off operation [73]. It has become very popular for high-power base-station PAs [74], but unfortunately less optimal to realize as an integrated amplifier. It consists of two or more linear PAs, and produces high output power with better efficiency over a wider output power range compared to a single linear class-AB amplifier, while not being so linear. A few integrated Doherty CMOS PAs have been published [75], [76].

The switched amplifiers generally have better back-off efficiency characteristics, as the additional methods needed for amplitude modulation will usually also improve efficiency at lower output power levels.

C. Circuit Solutions

The most common way to extend the tolerable supply voltage using low-voltage CMOS technology is to use the cascode or stacked transistor structure [77], [78], which in combination with thick-oxide transistors allows operation at higher supply voltage while keeping reliability at a high level. The result is higher output power, higher load, and lower current, which potentially leads to lower losses and higher efficiency. The output impedance is also higher compared to single common-source stage. The common configuration is shown in Fig. 5. The lower transistor, M1, is driven by the input signal in a common-source configuration. The upper transistor, M2, is usually connected to the supply voltage V_{dd}. M2 operates common gate (gate grounded) at high frequency because of the additional capacitor C_{LARGE}.

Under large-signal operation, the voltage will not be evenly distributed over the devices; the voltage swing on the gate–drain of M2 becomes larger than that of M1 [79]. M1 can therefore be selected for low-voltage operation, e.g., a thin-oxide standard transistor with better RF performance/gain, whereas M2 is selected for higher voltage operations, which can be a thick-oxide I/O transistor with longer channel length, typically 0.35–0.6 μm. As a thick-oxide I/O device does not have the same RF performance as a thin-oxide standard device, it will limit the RF performance of the amplifier stage. The width of the cascode transistor must be large enough to not degrade the linearity, but at the same time not too large to have a significant impact on the input or output matching. When the technology is scaled, but if PA supply voltage is kept constant, M2 needs to remain essentially the same, thus, performance of this structure will not improve with technology.

By using self-biasing [80], the supply voltage can be evenly distributed over the two devices. Two similar devices (high performance or high breakdown) can then be used, giving larger design space for voltage swing, reliability, and performance.

In switched PA architectures, the output power, efficiency, and gain become a function of the supply voltage. At lower supply voltages, the linearity and efficiency drop because the voltage applied at the gate of the M2 device is insufficient, and hence, M2 turns off. By biasing the M2 gate using a variable gate supply voltage, this problem can be solved [82].

By connecting several devices in series, stacking them, and biasing them properly, in principle n devices can handle n times the supply voltage, and the load resistor can be made $n*n$ times as high to achieve the same output power [83]. These structures are sometimes known as a high-voltage/high-power (HiVP) device configuration, [81], [84], Fig. 6, appearing mostly as non-integrated solutions. Variations of this concept can be found in [85]–[92], and has also been used with bipolar technology [93].

Operating points have to be carefully selected so that the devices operate optimally with good headroom; otherwise there is no performance gain. The cascode's gain is larger; therefore stabilization networks (e.g., an *RC*-link between gate and drain of M1) may be needed to reduce the risk of oscillations.

D. High-Breakdown Devices in Standard CMOS Processes

Another way to operate at high supply voltages is to use high-breakdown CMOS-compatible RF devices. Lateral double-diffused MOS (LDMOS) transistors have proven to be successful in base-station applications [94], [95]. The advantages of LDMOS for RF PA applications are its thermal stability, high ruggedness, and good linearity characteristics.

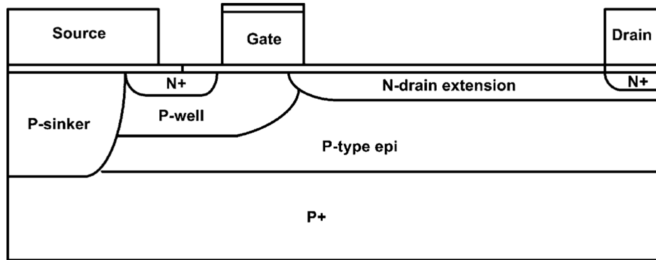

Fig. 7. Conventional LDMOS device.

LDMOS discrete devices typically operate between 24–50 V and can deliver up to 50 dBm of output power at 2 GHz. LDMOS devices are expected to be used up to 5 GHz [96]. A cross section of a typical discrete device structure is shown in Fig. 7. LDMOS devices have also been used for cellular handset PAs [34], [97].

LDMOS devices can be added to a conventional CMOS process with only a few extra masks and process steps. (We will use the term LDMOS for all these structures, although most of them are not strictly "laterally diffused," rather extended drain structures, EDMOS). An overview, also covering non-RF structures, is given in [98]. Early work concentrated on drift-region optimization by the reduced surface field (RESURF) technique [99], requiring process changes and additional masks. For these structures, the on-resistance can be minimized while still maintaining high breakdown voltages [100]. Recent examples of process extensions to form CMOS-compatible LDMOS devices can be found in [101]–[103].

LDMOS devices can also be added using layout and design environment changes with no added masks or other process changes. This is attractive to CMOS foundries thus not risking any change of the device parameters of existing CMOS devices. However, optimal performance (breakdown voltage, on-resistance, parasitics) will not be achieved in this way. Examples of LDMOS in CMOS foundry processes can be found in [104]–[109]. A number of CMOS foundries are today offering LDMOS or EDMOS devices into their RF-CMOS processes, but detailed information is sparse or confidential.

Conventionally, PAs are designed with n-devices because of their better RF performance compared to p-devices. However, for certain PA designs, such as switched class-D PAs, there is also a need for high-performance p-type RF devices. Examples of implementations of high-performance LDMOS p-devices can be found in [101], [103], and [110] using additional process steps, and [111] without process/mask changes.

To summarize this section, there are several methods to handle high voltages for PAs. Most of the recently published watt-level PAs (Section V) use cascode structures to enable safe operation at reasonable supply voltage.

III. Strategy: Load and Power Combination

A. Introduction

According to (1), the second parameter affecting the output power is the load. Although we could select a load impedance of e.g., 20 Ω to interface to our PA, it is common to use 50 Ω as a reference load between components such as the transceiver, switches, filters, and the antenna. To deliver 33 dBm (2 W) into a 50-Ω load (e.g., the antenna) at 3.3-V supply voltage, we need a load of $\sim$ 2.7 Ω. An impedance transformation network is used to transform the smaller load impedance of the PA to 50 Ω. As the transformation ratio ($50\ \Omega/Z_{\rm load}$) increases, the losses in the transformation network itself increase as the network has a finite Q [112].

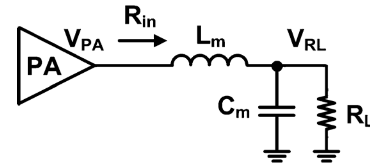

Fig. 8. Common L-match network to increase the power delivered to the load [112].

Simple narrowband transformation networks are usually resonant LC, Fig. 8, or transformer networks. For on-chip elements, especially for large L, the losses can be quite high and therefore LC output matching is often placed outside the chip on the printed circuit board (PCB). The L may then consist of part of the PCB conductor pattern, while the C often is a surface mount device (SMD). The obtained match is rather narrowband; 100 MHz (5% of the total band) is a typical number for a 2-GHz 27-dBm PA using such a first-order LC-network.

The simplest way to reach higher output power, or better matching, is to use differential PA structures, which will be discussed in Section III-B. Transformers can simultaneously be used for impedance-transformation power-combining baluns for differential PAs, and bias feeds. Considerable effort has therefore been made to optimize the structures and layout to integrate them with the PAs. This will be discussed in Section III-C.

B. Differential PA

By increasing the size of the PA output transistor, power is increased accordingly, but the impedance scales equally to lower values and we soon reach a point where the impedance is too small to conveniently be transformed to 50 Ω. The easiest way to further increase the output power for a given load is to use a differential structure [113]. The signal is split into two antiphase paths using a balun or transformer, two similar PA (half-size) blocks are used, and the signal is merged at the PA output using the same technique. If the transmitter architecture is differential, then the signal can be fed directly to/from the PA.

With this structure, we can gain a factor of four in the impedance for a given power, or have (up to) four times the output power for a given load. In practice, there are losses in the splitting and merging elements, but this is still an easy way to achieve higher output power.

The differential structure features a virtual ground, which makes it robust against parasitic inductance from the bondwires and leads to a good cancellation of even harmonics. Most of the switching currents will be internal currents between the two PA blocks, which are easier to handle than high currents to an external ground. In this way, the structure is important for the PA integration since it reduces the disturbance to other building blocks from large PA signals.

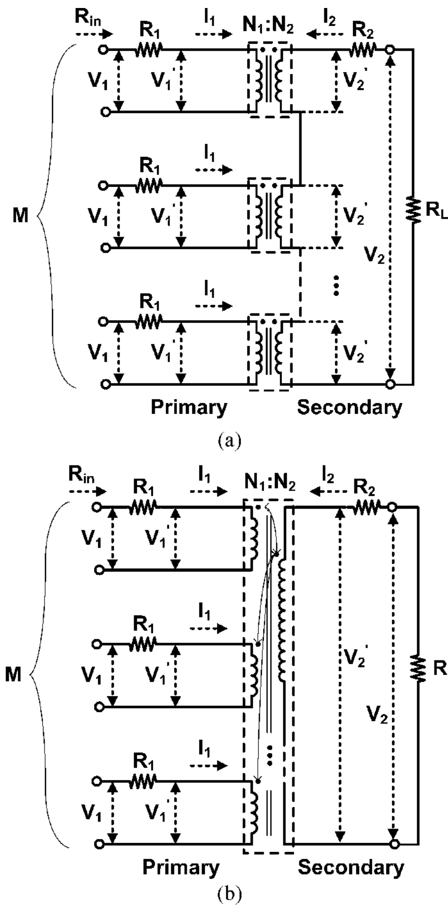

Fig. 9. Power combining transformers. (a) Series. (b) Parallel [114].

C. Power Combination Using On-Chip Transformers

Amplifiers operated differentially can be combined using an *LC* balun [115] and the concept can be extended to n elements, but this strategy is better aimed to increase efficiency as power is increased quadratically with the number of elements, but impedance linearly [83].

Instead, the key to really high output power for CMOS PAs is power combination using on-chip transformer structures. Considerable effort has been made to optimize the structures and layout to integrate them with the PAs. For a given transformation ratio, the transformers store less energy in the inductance compared to an *LC* matching network, resulting in lower loss for a given Q [18].

Transformer combination structures can be categorized as series-combining transformers (voltage mode) or parallel-combining (current mode) transformers, according to their ways of combining at the load [114], [116], Fig. 9. For the series combining, the secondary coils of n transformers are connected in series, the ac voltages add on the secondary side, generating higher output power. Impedance seen by each amplifier is n times larger compared to being connected directly to the load, which is advantageous for the driver design, and also for reducing the parasitic from the layout on the primary side. Care must be taken to obtain as much symmetry as possible, otherwise mismatch, which reduces the maximum output power and efficiency, will occur [117], [118].

Aoki *et al.* [11] used series combining to achieve the first implementation of a single-chip watt-level CMOS-PA with integrated input and output matching. The series-combining DAT architecture [18] serves as both a power combiner and matching network and can provide a solution with high efficiency, but occupies a relatively large chip area. By using transformers with different sizes, Javidan *et al.* [119] were able to shrink the area while still showing good performance. In examples of series power combination [120], [121], 1:1 transformers were used to combine the output of several amplifiers. Since each transformer can be independently switched off, it can also be used for power control.

The signal may also be parallel combined, which results in lower losses on the secondary side and provides better signal symmetry, as demonstrated in [116]. However, the number of turns with this approach becomes larger on the secondary side, increasing the area and lowering the self-resonance frequency. Other examples can be found in [122] and [123].

To summarize this section, what has proven to be the key to really high output power for CMOS PAs is power combination using on-chip transformers. Most of the recently published watt-level PAs (Section V) use different variants of on-chip transformer power combination.

IV. PA Reliability Concerns

A key factor behind the success of CMOS devices is the reliable operation of the devices, but this is only achieved at low supply voltages and within specified voltage ranges across the device terminals. This increases the design challenges in circuits with large voltage swings, such as PAs, to achieve the desired output power while still having an acceptable lifetime. The reliability design rules in foundry design manuals do not commonly address the case of large-swing PAs operation, with voltage peaks well above the supply voltage only for a short part of the switching cycle at gigahertz frequency. Simulations of internal device node voltages and stress measurements on fabricated devices can be used to explore actual limits. The specific circuit configuration and the use-case for the product are important factors for final design considerations [124].

The lifetime of MOS transistors depends mainly on the vertical and lateral electric field in the transistor and across junctions. PA lifetime translates mainly to voltage stress over time (high, but short voltage peaks), and only over certain device nodes. Electromigration and thermal issues can often be handled by good layout practices. The actual PA failures will typically be drift in performance parameters, such as reduced output power over time. Catastrophic failures, such as gate–oxide breakdowns or junction burnouts, can usually be avoided.

The three main device lifetime-determining mechanisms are: 1) gate oxide breakdown; 2) hot-carrier stress; and 3) junction breakdown.

Gate–oxide breakdown is catastrophic and must under all situations be avoided. This will set limits for the gate-to-source, gate-to-substrate, and the gate-to-drain voltages. High electrical field over the gate will over time lead to catastrophic breakdown, known as time-dependent dielectric breakdown (TDDB). A common practice is to keep the maximum voltage drops across the devices below two times the supply voltage

TABLE II
COMPARISON OF STATE-OF-THE-ART FULLY INTEGRATED RF CLASS-AB LINEAR PAs

Ref.	Year	P-1dB [dBm]	Psat[a] [dBm]	High-power approach[b]	V_{DD} [V]	PAE [%]	f [GHz]	tech node [nm]	BW [GHz]
[118]	2009	28.5	30.1	casc/series tr	3.3	33	2.4	90	0.7[c]
[128]	2012		30.5	casc/other tr	3.4	42.1	1.95	180	0.3[d]
[76]	2012		30.5	casc/Doherty	3.3	34	2.4	65	-
[87]	2010		31	casc/stacked	3.6	60.5	0.85	65	0.17[d]
[129]	2011	28	31	casc/para tr	3.3	34.8	2.5	180	-
[130]	2009	27	31	casc/para tr	3.3	27	2.4	180	-
[131]	2010	27.5	31.5	casc/LC	3.3	25	2.45	65	0.8[c]
[132]	2006		31.5	casc/Doherty	3.3	36	1.7	130	-
[133]	2010		32	casc/other tr	3.3	48	2.2	90	>1.4[d]
[90]	2010	30.8	32.4	stacked	6.5	47	1.9	130 SOI	-
[134]	2013	32.8		high V_{dd}	3.3	52	2.4	65[e]	-
[18]	2008		33	casc/DAT	3.5	45	1.9	130	-
[116]	2010		33.5	casc/para tr	3.3	37.6	2.4	65	2[c]
[18]	2008		35	casc/DAT	3.5	51	0.9	130	-

[a] Psat assumed if not stated otherwise.
[b] casc=cascode, stacked=more advanced/different than cascode, series tr=series transformer combiner, para tr=parallel transformer combiner, other tr = other type of transformer combiner, LC = distributed LC combiner, DAT = distributed active transformer [11].
[c] 3 dB bandwidth.
[d] 1 dB bandwidth.
[e] LDMOS device (no process changes).

TABLE III
COMPARISON OF STATE-OF-THE-ART INTEGRATED RF CLASS-E SWITCHED PAs (NO AMPLITUDE MODULATOR INCLUDED)

Ref.	Year	Peak P_{out} [dBm]	High-power approach[a]	V_{DD} [V]	DE [%]	PAE [%]	f [GHz]	tech node [nm]	BW[b] [GHz]
[138]	2009	30.2	casc/para tr	3.3		36.8	1.55	180	0.2
[92]	2013	30.3	stacked/other tr	6.35		17.8	5.3	65	1.9
[139]	2011	31	high V_{dd}	5	77	65	0.7	65[d]	0.6
[114]	2008	31.2	casc/para tr	3.3		41	1.8	180	0.2
[140]	2010	31.5	casc	3.5	54	51	1.8	130	0.5
[141]	2007	31.5	casc/DAT	3.3		41	1.8	180	0.5
[142]	2007	32	casc/other tr	3.3		40	1.8	180	0.2
[114]	2008	32	casc/para tr	3.3		30	1.8	180	0.2
[143]	2008	32.2	casc/DAT	3.3	35.6		1.88	180	0.3
[123]	2007	33	casc/para tr	3.3		30	1.8	180	0.3
[11]	2001	33.4	DAT	2		31	2.4	350	0.51[c]
[144]	2009	33.8	casc/para tr	3.3		50	1.8	180	0.2
[145]	2007	33.5	casc/DAT	3.3		41	1.8	180	0.4
[146]	2009	35.3	high V_{dd}	6		59	2	65[d]	-

[a] casc=cascode, stacked=more advanced/different than cascode, para tr=parallel transformer combiner, other tr = other type of transformer combiner, DAT = distributed active transformer [11].
[b] 1 dB minimum bandwidth estimations from data in papers.
[c] 3 dB bandwidth.
[c] LDMOS device (no process changes).

so that the field across the oxide never exceeds the breakdown field of $\sim$ 1-V/nm gate oxide [79], [124]. The impact of oxide RF stress is not as damaging as dc stress [125]. During RF operation, the TDDB is proportional to the root mean square (rms) value of the electric field over the gate oxide [126].

Hot-carrier stress, or more specific high-voltage gate-to-drain stress, will generate high-energy "hot" carriers tunneling through the gate oxide. Some of them will be trapped in the oxide, which will change the threshold voltage and transconductance, degrading the device performance. The hot carriers may also result in avalanche multiplication and surface defects, which will cause reduced carrier mobility in the channel. For devices with $L > 100$ nm, hot-carrier stress is most severe when drain–source voltage is high ($> =$ maximum rated supply voltage) and gate–source voltage is around half the drain–source voltage. For devices with $L < 100$ nm, maximum stress occurs when gate–source voltage is similar to the drain–source voltage [124].

Junction breakdown, including source–drain punch-through, may not directly be a destructive phenomenon compared to gate–oxide breakdown and hot-carrier stress. However, large current and large voltage drop across devices may result in hot carriers and thermal problems, especially if applied for a long period of time.

Depending on the circuit configuration, the voltage stress across the device nodes varies. It varies also during the switching cycle and only a small part of the cycle consists of high-stress conditions. Linear class-A/B/C PAs have a significant voltage across the device while conducting current, which creates mainly hot-carrier stress. Switching class-D amplifiers behave like digital inverters with all node voltages smaller than the supply voltage, thus the stress is comparatively low [127].

TABLE IV
COMPARISON OF STATE-OF-THE-ART FULLY INTEGRATED RF OUTPHASING PAs

Ref.	Year	Output PA class	Peak P_{out} [dBm]	High-power approach[a]	V_{DD} [V]	DE [%]	PAE [%]	f [GHz]	tech node [nm]	BW[b] [GHz]
[147]	2011	D	30.5	casc/series tr	6.0	29.7	26.5	1.95	65	1.60
[148]	2012	D	31.5	casc/series tr	2.4		27.0	2.4	45	1.70
[47]	2011	D	32.0	casc/series tr	5.5	20.1	15.3	1.85	130	0.90

[a] casc=cascode, series tr=series transformer combiner.
[b] 3 dB bandwidth.

Class-E switching amplifiers have only a small voltage drop across the transistor when it conducts current, resulting in low hot-carrier stress. However, when a class-E amplifier is in off-state (gate at ground), the drain voltage may peak at values up to 3.5 times the supply voltage, creating a high field at the oxide edge between the gate and the drain [79], [135].

The recommended maximum operating voltage in design manuals to avoid hot carrier degradation is usually based on dc/transient reliability tests. Values may be different for specific PA product use-cases, and stress measurements may be useful. For hot-carrier stress, most of the degradation occurs during the first few hours. In [136], a test was made using a supply voltage of 90% of the limit for the used technology. The output power of the amplifier decreased in the order of 1 dB after 70–80 h of continuous operation, which was considered to be acceptable. In [124], a test time of 168 h at elevated supply voltage was considered to cover more than five years of reliable product use for the WLAN. The required lifetime should be put in relation to the employed standard and expected use case [137]. A GSM mobile phone used for 4 h a day during 18 months corresponds to only 275 h of continuous PA operation since 2G GSM has a 12.5% duty cycle)

V. STATE-OF-THE-ART PAs

In this section, state-of-the-art integrated CMOS PAs with peak power greater than 30 dBm are listed and compared. The PAs incorporate most or all of the passive matching and biasing components by utilizing integrated capacitors, inductors, or transformers. A few multi-chip or module PAs have also been included.

Linear PAs are listed in Table II. They provide a more or less complete amplifier on a chip, contrary to the switched class-D and class-E amplifiers, which need additional circuitry to perform amplitude modulation (Section II-B).

As pointed out in Section II-B, class-D amplifiers require fast p-devices, which have not been available until about the 130-nm CMOS node and we have not found any published separate CMOS class-D PA cores with watt-level output, however many class-E PA cores, listed in Table III. (We use the term "PA core" for switched PAs without the additional circuitry for amplitude modulation.)

Fully integrated outphasing PAs, including modulation circuitry, are listed in Table IV. They are very recent and based on class-D PA cores.

Polar modulated PAs, including the modulation circuitry, are listed Table V. They are mostly based on class-E cores and no circuit in Table V is a true single-chip integrated PA.

From the tables, we can observe that there are many examples of CMOS class-AB PAs with saturated output power larger than 1 W at 1–2.5 GHz. Fully integrated switched PAs with amplitude modulation have only been demonstrated using class-D cores in outphasing architectures.

To gain more insight on how to reach watt-level output power with actual integrated PAs, the different approaches used to achieve high output power are indicated in the tables. From this, we make the following observations.

1) The PA should be operated at as high a supply voltage as possible. This is achieved using cascode or stacked structures. Almost all of the surveyed PAs, in different classes, are designed in this way. For linear class-A/B/C and switched class-E with peak switching voltages of 2–3.5 times V_{dd}, the PA can be operated reliable at the higher supply voltage (3.3 V) usually available in the system. For the switched class-D, with no overvoltage, cascodes make it possible to operate the PA at increased supply voltage with low-voltage transistors. In this aspect, the class-D architecture may be best suited for use with low supply voltage, e.g., early designs in the new technologies where no additional devices for analog/mixed-signal design yet have been added. But the output power at a given supply voltage is lower for the class-D compared to the linear classes (Table I).
2) High output power is achieved by using large parallel device structures. As the impedance will get too low to match directly to the ubiquitous 50-Ω output, almost all surveyed PAs use on-chip power-combining transformers, with the parallel approach as the dominating solution.
3) The switching transistor classes need to be used with architectures that provide output power modulation. Although the class-E switched PAs have drawn much research interest lately with (or at least aimed for) polar modulation, the highest demonstrated output power with CMOS integrated PAs have been achieved using class-D amplifiers and outphasing architecture.

Finally, when studying Table II–V, the reader will notice the spread in peak efficiency for different PAs of the same class. What sets the actual efficiency is a combination of PA class, architecture, device operating point, and ultimately losses, both in the circuit and any external matching network. For multi-stage PAs, the properties of the output stage will dominate. As the results in the tables range from research-level device-only raw performance, to complete multi-stage circuits with a high degree of integration, there is a natural spread in the performance parameters.

TABLE V
COMPARISON OF STATE-OF-THE-ART INTEGRATED RF POLAR-MODULATED PAs

Ref.	Year	Output PA class	Peak P_{out} [dBm]	High-power approach[a]	V_{DD} [V]	PAE [%]	f [GHz]	tech node [nm]	BW[b] [GHz]
[68][c]	2012	D	30	stacked/Guanella	3.3	40.6	0.75	150	0.2
[21][d]	2009	E	32.5	casc/para tr	3.4	52	1.8	180	0.2
[149][b]	2012	E	33[e]	casc	3.5	34	1.8	180	-
[21][d]	2009	E	34.5	casc/para tr	3.4	55	0.9	180	0.2
[19][f]	2011	E	34.5	casc/para tr	3.0-4.2	55	0.9	180	-

[a] casc=cascode, stacked=more advanced/different than cascode, Guanella = Guenella reverse balun, para tr=parallel transformer combiner.
[b] 1 dB minimum bandwidth estimations from data in papers.
[c] Multi-chip. PWM modulated.
[d] Module.
[e] Estimated (26 dBm av., 7.5 dB PAPR, low EVM).
[f] Output parallel transformers on separate low-loss substrate.

VI. CONCLUSIONS AND FUTURE PROSPECT

This paper has presented a review and state-of-the-art compilation of watt-level integrated CMOS PAs.

Two strategies to reach watt-level output have been identified: the use of high supply voltage, and the use of matching/power combination (high current). When using foundry CMOS processes with few special options for RF and PA design, the designer needs to combine several features to reach watt-level output power.

Standalone CMOS-PAs that compete with today's GaAs-based PA modules are less attractive in our view, although they probably can find a niche for low-cost products. The long-term driving force for the integrated PA, or even "the Holy Grail of the RF CMOS quest" [6], is the full integration of digital, analog, radio, and PA into a SoC single-chip radio in CMOS.

Watt-level standalone linear PAs both for 2G and 3G cellular are (almost) off-the-shelf technology today. Although much research has been done in this area during the last decade, fully integrated switched PAs (with potentially higher efficiency) have only appeared quite recently (Table IV). The outphasing architecture using class-D PA core has not widely been accepted as a good solution. For the popular class-E-based PA using variants of polar modulation/envelope tracking, we have not found any publications of fully integrated PAs; the design of an integrated modulator with high bandwidth and low losses in CMOS appears to be the weak point.

Watt-level integrated RF-PAs are achievable, but it will take some more years before we see demonstrations that can be completely integrated with the CMOS transceiver. There is still room for novel architectures that can utilize the large number of transistors available in CMOS almost for free, but also handle the limitations from low supply voltage and lossy substrate and passives, to achieve the ultimate goal of the fully integrated CMOS transceiver.

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