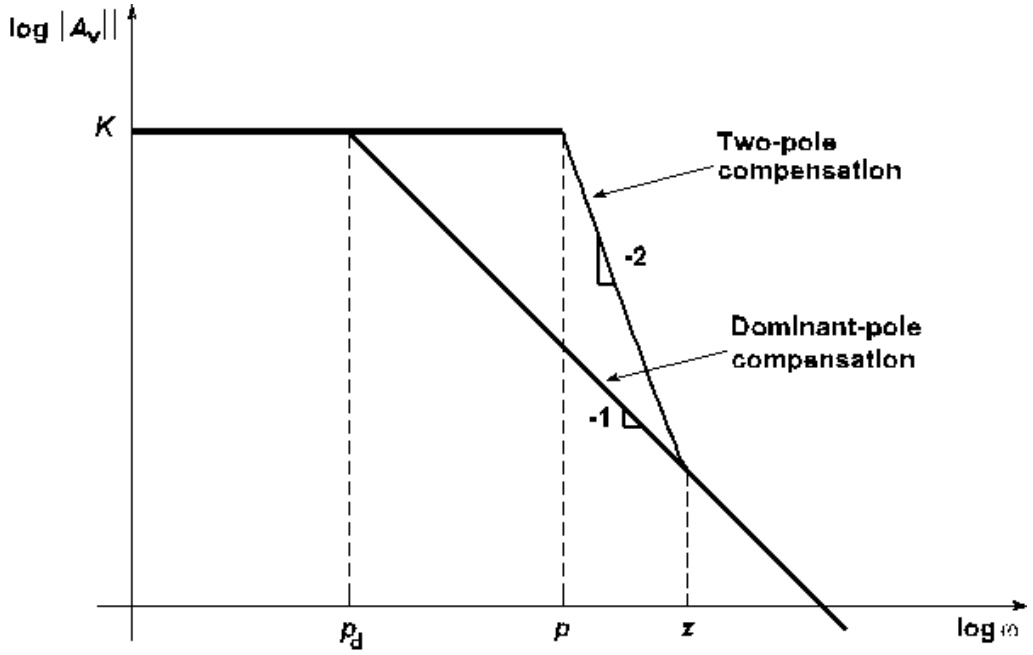
Two-Pole Compensation

Part 1: Basic Two-Pole Compensator

by Dennis L Feucht

High-performance feedback amplifiers require high loop gain over a wide frequency range. Dominant-pole (single-pole) compensation reduces gain appreciably at higher frequencies because the pole must be placed at a relatively low frequency in order to decrease the loop gain to one at a desirable phase margin. The dynamic response may then be acceptable but the side-effect is that, except at low frequencies, the loop gain rolls off, and high-frequency amplifier performance suffers. The benefits of feedback are retained by keeping the loop gain high over the frequency range of interest. If loop gain is too low at higher frequencies, then distortion (or nonlinearity) is high and noise rejection low. For an ADC interface, bits of accuracy and SNR will be lost at higher frequencies, and for the audiophile, the cymbals will sound "tinny."

The *two-pole compensation* technique sustains high gain to a higher break frequency, where it then rolls off at −40 dB/decade (−2 slope) followed by a zero that restores the magnitude to that of dominant-pole compensation. The difference is shown in the Bode magnitude plot below.



The high loop gain is extended from the dominant-pole break frequency at p_d to p, where two poles reside. The gain then decreases with a −2 slope to z, the frequency of the zero. Above z, the response follows the dominant-pole response, with a −1 slope. The zero restores the phase margin lost by the additional pole.

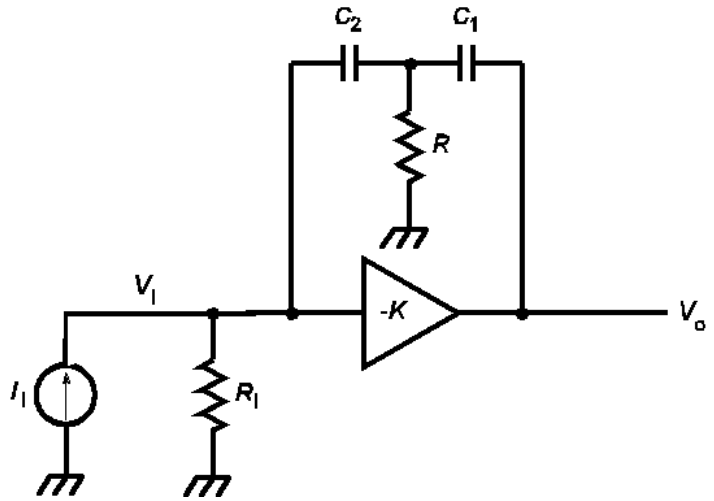
The above Bode plot can be expressed algebraically by the generic voltage-gain transfer function:

$$\frac{V_o}{V_i} = \frac{s/z+1}{as^2+bs+1} = \frac{s/z+1}{(s/p+1)^2} = \frac{s/z+1}{\left(\frac{s}{\omega_n}\right)^2 + \left(\frac{2\cdot\zeta}{\omega_n}\right)\cdot s + 1}$$

where, ω_n is the pole radius and ζ is the damping ratio. For $\zeta = 1$, the pole pair is critically damped and the two poles are equal, at p. The pole angle is $\cos^{-1}(\zeta)$ for $\zeta \le 1$. We will assume identical, real poles for now.

Two-Pole Compensator Circuit

A typical two-pole-compensator amplifier circuit is shown below.



For the ideal op-amp, static (dc) gain, *K*, is infinite, and the compensation poles reside at the origin -- a dominant-pole amplifier. As one stage of a feedback amplifier loop, however, *K* can be finite. From the Bode plot above, as frequency increases, the reactance of the capacitors decreases relative to *R* until $X_C << R$. Then the equivalent circuit consists of the two capacitors in series, shunting the op-amp. The series capacitance forms an op-amp integrator with a dominant-pole response. The zero of the circuit is located at the frequency for which *R* becomes negligible relative to X_C. At the zero, the frequency response breaks from a slope of −2 to −1. The above circuit has a loop gain of:

$$GH = K \cdot \frac{s^2 RR_i C_1 C_2}{s^2 RR_i C_1 C_2 + s(RC_1 + RC_2 + R_i C_2) + 1}$$

where, $G = -K$. The closed-loop voltage gain includes a pre-loop transfer function of:

$$T_i = R_i \cdot \frac{sR(C_1 + C_2) + 1}{s^2 RR_i C_1 C_2 + s(RC_1 + RC_2 + R_i C_2) + 1}$$

and is:

$$\frac{V_o}{V_i} = T_i \cdot \frac{G}{1 + GH} = -K \cdot \frac{sR(C_1 + C_2) + 1}{s^2 RR_i C_1 C_2 (K+1) + s(RC_1 + RC_2 + R_i C_2) + 1}$$

where, $V_i = R_i \cdot I_i$. For an ideal op-amp, $K \to \infty$, and the voltage gain becomes:

$$\frac{V_o}{V_i}\Big|_{K \to \infty} = -\frac{sR(C_1 + C_2) + 1}{s^2 RR_i C_1 C_2}$$

As *K* increases, the quadratic term in the closed-loop voltage gain dominates, shifting the poles to the origin. This results in loop-gain rolloff from 0 Hz, defeating the two-pole compensator. Consequently, the above circuit can be used as a two-pole compensator under the condition that *K* remains finite. The two-pole compensator, with its poles far removed from the origin, cannot use the open-loop gain of an op-amp for *G*.

Another simplification of the circuit is to let $R_i \to \infty$. This is the case of a transimpedance amplifier with input I_i. Its transresistance is:

$$\frac{V_o}{I_i}\Big|_{R_i \to \infty} = -K \frac{sR(C_1 + C_2) + 1}{sC_2[s(K+1)RC_1 + 1]}$$

The pole dependent upon R_i moves to the origin. Without a finite R_i, the poles cannot be equal and two-pole compensation is not realized under this condition either.

As $R \to \infty$, the voltage gain becomes:

$$\frac{V_o}{V_i}\Big|_{R\to\infty} = -K\frac{1}{sR_i(C_1 \| C_2)(K+1)+1}$$

With R open, the circuit defaults to dominant-pole compensation. (The factor $C_1 \parallel C_2$ is the series combination of C_1 and C_2; $\parallel$ is denotes the mathematical "parallel" operation, and is not a topological descriptor.) In addition, with an ideal op-amp, as $K \to \infty$, the pole approaches the origin and the gain is:

$$\frac{V_o}{V_i}\Big|_{R,K\to\infty} = -\frac{1}{sR_i(C_1 \| C_2)}$$

This is a dominant single-pole amplifier response with an amplifier shunt capacitance of C_1 and C_2 in series.

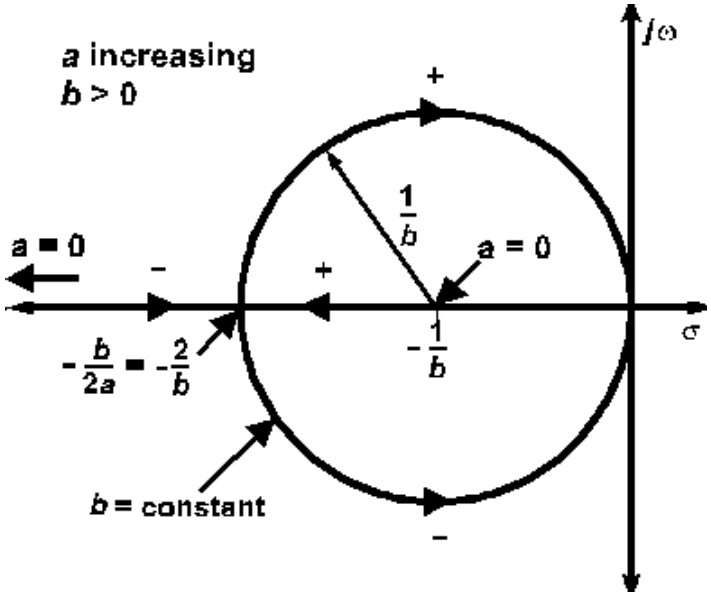
Two-Pole Compensator Design Constraints

The above algebraic expressions for closed-loop gain do not of themselves satisfy the requirements for two-pole compensation. The following conditions must also hold:

- The poles must be equal (or close): $p_1 = p_2 = p$
- The poles must be less than the zero: $z/p > 1$
- The first condition is satisfied for real poles when the coefficients of the quadratic pole factor of the closed-loop voltage gain have the relation:

$$a = \left(\frac{b}{2}\right)^2$$

where, a is the quadratic coefficient and b is the linear coefficient. Under the above condition, the quadratic polynomial factors into a perfect square. Because the $K + 1$ factor is in a only, its variation produces the loci of poles for a constant b, shown below.



The poles are equal when their value is $-b/2a$, and the corresponding gain is found by setting the discriminant, $b^2 - 4a$, to zero and solving for $K + 1$:

$$K+1\Big|_{p_1=p_2} = \frac{R^2(C_1+C_2)^2 + 2R_iR(C_1+C_2)C_2 + R_i^2C_2^2}{4R_iRC_1C_2}$$

K is a finite amplifier open-loop gain that can be implemented as an op-amp inner-loop fixed-gain stage. But this requires additional circuitry and the feedback network that sets the gain of the op-amp must not interfere with the two-pole feedback network. The two-pole circuit is usually made to be one of the stages in the forward path (G) of a feedback amplifier, within a larger loop.

Instead of setting the compensator by adjusting K, solve the $K + 1$ equation above for one of the compensator elements, R:

$$R = \frac{R_iC_2}{(C_1+C_2)^2}[(2K+1)C_1 - C_2 \pm 2\sqrt{C_1(K+1)(KC_1-C_2)}]$$

where, $p_1 = p_2$ and, of course, R is positive and real, requiring that $KC_1 > C_2$. This rather involved equation can be simplified by approximation to:

$$R \cong R_i\left[\frac{4K(C_1 \| C_2)}{C_1+C_2}\right], \qquad K >> 1, \qquad KC_1 >> C_2, \qquad p_1 = p_2$$

The second constraint on two-pole compensator realization is that $z > p$. From the closed-loop voltage gain:

$$z = \frac{1}{R(C_1+C_2)} = \frac{1}{\tau_z}$$

and the positive value of the two poles is:

$$p = \frac{b}{2a} = \frac{R(C_1+C_2)+R_iC_2}{2R_iRC_1C_2(K+1)} = \frac{1}{\tau_p}$$

Because the poles are equal, $a = (b/2)^2$, and both poles are located (as shown on the above root-locus plot) on the real axis at:

$$\frac{b}{2a} = \frac{2}{b}$$

Then the condition $z > p$ becomes:

$$\frac{1}{\tau_z} > \frac{2}{b} = \frac{1}{\tau_p}$$

But from the voltage-gain expression, $b = \tau_z + R_i C_2$. Substituting:

$$\frac{1}{\tau_z} > \frac{2}{\tau_z + R_iC_2} = \frac{1}{\tau_p}$$

or,

$$R_iC_2 > \tau_z = R(C_1+C_2)$$

If we solve for R_iC_2 in terms of (z/p), we get the equality:

$$R_iC_2 = \tau_z\left(2\cdot\frac{z}{p}-1\right)$$

By solving $z > p$, using $b/2a$ instead of $2/b$, we get:

$$R_iC_2 = \frac{z}{p}\cdot\frac{\tau_z}{2(K+1)[C_1/(C_1+C_2)]-z/p}, \qquad \frac{z}{p} < 2(K+1)\left(\frac{C_1}{C_1+C_2}\right)$$

The additional constraint on z/p is weak for large K but suggests that $K\cdot C_1$ be made larger than C_2 for maximum pole-zero separation. A special case of this equation is:

$$\frac{z}{p} \cong 2(K+1)\left(\frac{C_1}{C_1+C_2}\right), \qquad R_iC_2 >> \tau_z$$

When R_iC_2 dominates b, the pole-zero separation is pushed to the limits. In this case, with large K:

$$R \cong R_i\left[\frac{C_2}{4KC_1}\right], \qquad R_iC_2 >> \tau_z, \qquad K >> 1, \qquad p_1 = p_2$$

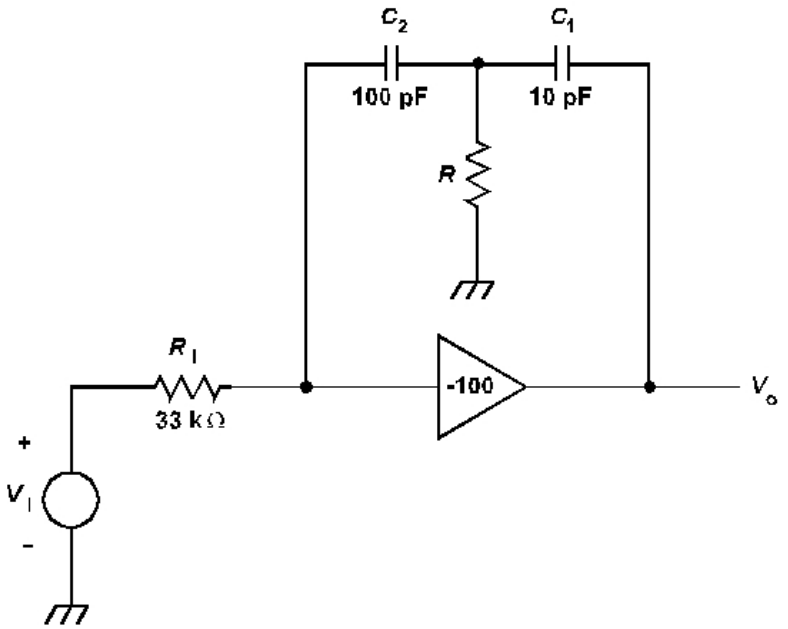
Finally, from the general expression for R_iC_2, the constraint on the capacitors is:

$$\frac{C_1}{C_2} < \frac{R_i}{R} - 1$$

With these formulae, we can design two-pole compensators, as we will take up in part 2. For now, we will analyze an example two-pole amplifier.

Two-Pole Compensator Circuit Example

A two-pole amplifier has the following circuit values:



$K = 100, \qquad R_i = 33\,\text{k}\Omega, \qquad C_1 = 10\,\text{pF}, \qquad C_2 = 100\,\text{pF}$

For this amplifier:

$$R = 33\,\text{k}\Omega \cdot \left[\frac{100\,\text{pF}}{4(100)(10\,\text{pF})}\right] = 825\,\Omega$$

$$\tau_z = R(C_1 + C_2) = (825\,\Omega)(110\,\text{pF}) = 90.75\,\text{ns}$$

and the conditions of:

$$R \cong R_i\left[\frac{C_2}{4KC_1}\right], \qquad R_iC_2 >> \tau_z, \qquad K >> 1, \qquad p_1 = p_2$$

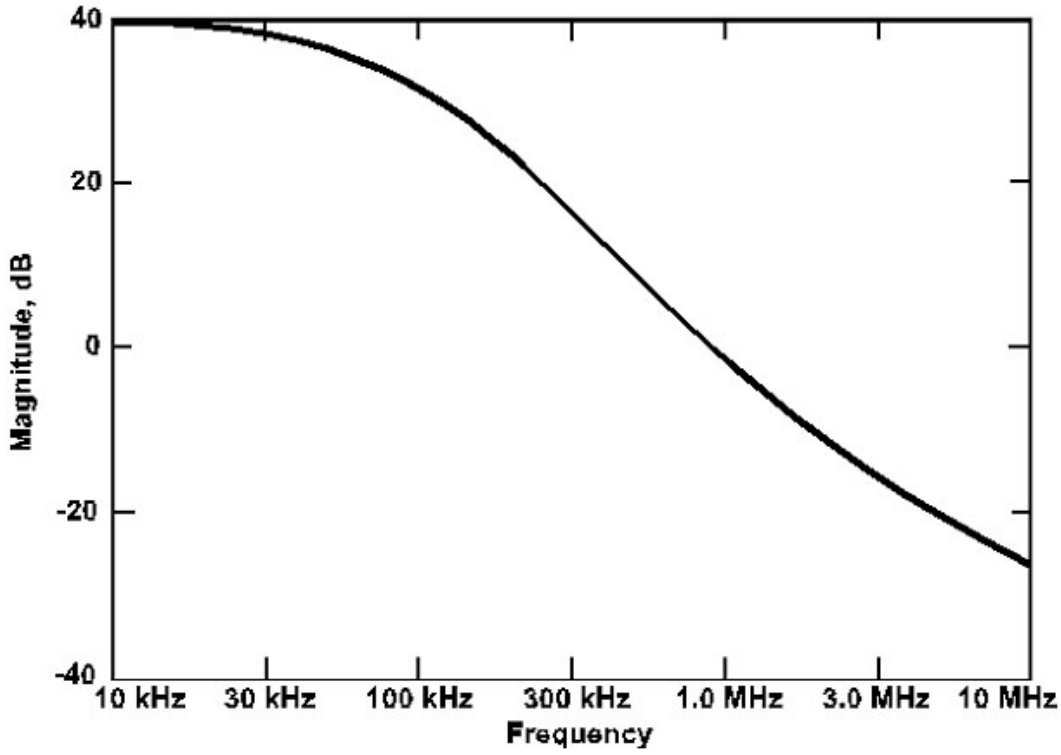
are satisfied. All element values are determined, and the natural frequency of the pole factor, which is the break frequency of the two poles, is found either from:

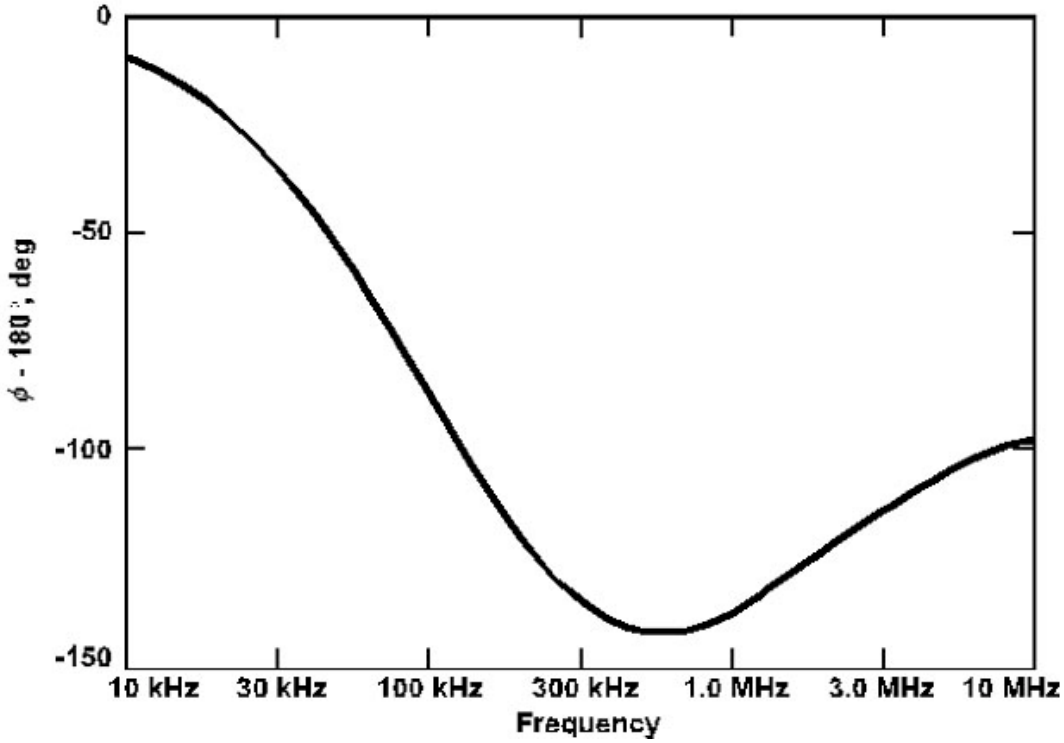
$$\frac{1}{\tau_z} > \frac{2}{\tau_z + R_iC_2} = \frac{1}{\tau_p}$$

or directly from *a*:

$$f_n = \frac{1}{2\pi\sqrt{a}} = \frac{1}{2\pi\sqrt{R_iRC_1C_2(K+1)}} = 96.5\,\text{kHz}$$

As a check, when the poles of a quadratic factor are equal, damping ratio, $\zeta = 1$. From the pole factor of the closed-loop voltage gain, $\zeta = b/2\sqrt{a} = 1.03$. The zero is located at $1/2\pi{\cdot}R(C_1 + C_2)$ = 1.75 MHz. From the SPICE simulation, the phase is –90° at 100 kHz, where the poles should be. The Bode plots from circuit simulation are shown below.





As a check, the magnitude will be down –6 dB (for two poles) at the break frequency. At 34 dB (down from a static (dc) gain of 40 dB), it is 91 kHz. The maximum closed-loop phase lag occurs at 631 kHz and is –142°. The non-monotonic phase plot, which dips down and comes back up due to the zero, is characteristic of two-pole-compensated amplifiers. The magnitude plot rolls off with a –2 slope at the pole frequency to the zero frequency at about 1.75 MHz. (Because the amplifier is inverting, the phase is offset by –180°.)

Closure

The design equations and constraints for a two-pole compensator circuit have been presented and a two-pole circuit example analyzed. This article will be continued in part 2, extended to the more general case of complex poles.

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