IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2017 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 5, 6, 7, 8, 9

CONFERENCE THEME:

INTELLIGENT CHIPS FOR A SMART WORLD

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: IC REGULATORS FOR SoC AND IoT; FREQUENCY GENERATION FOR WLs AND WLn

10 TUTORIALS: mm-WAVE SYNTHESIZERS; NAND FLASH TRENDS; PHYSIOLOGICAL-READOUT CIRCUITS; LOW-ENERGY PROCESSORS FOR DEEP LEARNING; TIME-BASED CIRCUITS; SIGNAL INTEGRITY FOR Gb/s LINKS; DIGITAL-INTENSIVE PLLS; CLASS-D AMPLIFIERS; IC mm-WAVE TX/RX SPATIAL FILTERING; CELL AND BRAIN INTERFACING

2 EVENING EVENTS ON GRADUATE STUDENT RESEARCH IN PROGRESS, INTELLIGENT MACHINES

THURSDAY ALL-DAY

4 FORUMS: FUTURE COMPUTATIONAL PARADIGMS; DEEP LEARNING TO NEUROMORHISM; WIRELESS TRANSCEIVERS FOR LAN/WAN; WIRELINE TRANSCEIVERS FOR MEGA DATA CENTERS AT/ABOVE 50Gb/s; PERFORMANCE LIMITS IN DATA CONVERTERS

SHORT-COURSE: ULTRA-LOW-POWER ANALOG DESIGN

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 5th, the day before the official opening of the Conference, ISSCC 2017 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, "Intelligent Machines: Will the Technological Singularity Happen" will be offered starting at 8:00pm. In addition, the Student-Research Preview, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Professor Hoi-Jun Yoo of KAIST, Daejeon, Korea.

On Monday, February 6th, ISSCC 2017 offers four plenary papers on the theme: "Intelligent Chips for a Smart World". On Monday at 12:15 pm, there will be a Women's-Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. Monday evening will include 2 events entitled "Quantum Engineering: Hype, Spin, or Reality" and "Semiconductor Economics: How Business Decisions Are Engineered".

On Tuesday, February 7th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled "Return of Survey Says!" and "When Will We Stop Driving Our Cars".

On Wednesday, February 8th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 9th, ISSCC offers a choice of five all-day events:

- A Short Course entitled "Ultra-Low-Power Analog Design"
- Four Advanced-Circuit-Design Forums entitled
  - "Beyond the Horizon of Traditional Computing: From Deep Learning to Neuromorphic Systems";
  - "Wireless Low-Power Transceivers for Local and Wide-Area Networks";
  - "Wireline Transceivers for Mega Data Centers: 50Gb/s and Beyond";
  - "Pushing the Performance Limits in Data Converters".

Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

TUTORIALS — Sunday February 5, 2017

mm-Wave Frequency Generation and Synthesis in Silicon
Payam Heydari, *University of California, Irvine, Irvine, CA*

NAND Flash Memory Design and Architecture Trend
Sungdae Choi, *SK hynix, Icheon-si, Korea*

Readout Circuits for Physiological Signal Measurements
Long Yan, *Samsung Electronics, Hwaseong-si, Korea*

Energy-Efficient Processors for Deep Learning
Marian Verhelst, *KU Leuven, Heverlee, Belgium*

Fundamentals of Time-Based Circuits
Matt Straayer, Maxim Integrated Products, North Chelmsford, MA

Signal Integrity Analysis for Gb/s Links
Tony Chan Carusone, *University of Toronto, Toronto, Canada*

Design Trade-Offs in Digital Intensive PLLs
Ping-Ying Wang, CMOS-Crystal, Hsinchu, Taiwan

Fundamentals of Class-D Amplifier Design
Xicheng Jiang, *Broadcom, Irvine, CA*

Integrated mm-Wave Transmitters and Receivers for Spatial-Filtering Array
Arun Natarajan, *Oregon State University, Corvallis, OR*

Circuits and Technologies for Cell and Brain Interfacing
Nick Van Helleputte, *imec, Heverlee, Belgium*

2 FORUMS — Sunday February 5, 2017

Integrated Voltage Regulators for SoC and Emerging IoT Systems

High-Performance Frequency Generation for Wireless and Wireline Systems

4 FORUMS — Thursday February 9, 2017

Beyond the Horizon of Conventional Computing: From Deep Learning to Neuromorphic Systems

Wireless Low-Power Transceivers for Local and Wide-Area Networks

Wireline Transceivers for Mega Data Centers: 50Gb/s and Beyond

Pushing the Performance Limit in Data Converters

EVENING EVENTS — February 5, 2017

Student Research Preview: Poster Session with Short Presentations

Intelligent Machines: Will the Technological Singularity Happen?

EVENING EVENTS — February 6-7, 2017

Monday: Quantum Engineering: Hype, Spin or Reality?
Semiconductor Economics: How Business Decisions are Engineered

Tuesday: When Will We Stop Driving Our Cars?
Return of Survey Says!

SHORT COURSE — Thursday February 9, 2017

Ultra-Low-Power Analog Design

MOSFET Modeling for Ultra-Low-Power Analog
Christian Enz, *EPFL, Neuchatel, Switzerland*

Integrated DC-DC Converters for Low-Power Applications: From Discrete Towards Fully-Integrated-CMOS Power Management
Michiel Steyaert, *KU Leuven, Leuven, Belgium*

Ultra-Low-Power References and Oscillators
Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

Micropower ADCs
Kofi Makinwa, *Delft University of Technology, Delft, The Netherlands*

HOW TO REGISTER FOR ISSCC

On line: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the registration website.
FAX, mail or email: The Registration Form can be downloaded from the registration website. Please read the descriptions and instructions on the back of the form carefully.
On site: The On-site Registration and Advance Registration pickup desks at ISSCC 2017 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis.
Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Sunday January 8, 2017.** After January 8th, and on or before 11:59 pm Pacific Time **Sunday January 15, 2017**, registrations will be processed **at the Late Registration rates. After January 15th, you must register at the on-site rates.**
IEEE and Solid-State Circuits Society members enjoy lower registration fees. Consider joining IEEE and SSCS before registering.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Starting Sunday evening and continuing through Wednesday.
Technical Book Display: Several technical publishers will have professional books and textbooks for sale during the Conference.
Demonstration Session: Hardware demonstrations will support selected papers.
Author Interviews: Author Interviews will be held after each day's sessions.
Social Hours: Social Hour refreshments will be available evenings.
University Events: Several universities are planning social events during the Conference.
ISSCC Water Bottle: A convenient water bottle for travel or sports will be given to all Conference registrants.
Digest of Technical Papers: In hard copy and by download.
Papers Visuals: The visuals from all papers presented will be available by download.
Demonstration Sessions Guidebook: A descriptive guide to the Demonstration Sessions will be available by download.

OPTIONAL EVENTS

Educational Events: Many educational events are available on Sunday and Thursday for an additional fee. The Forums and Short Course include meals.
Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits.

OPTIONAL PUBLICATIONS for SALE

ISSCC 2017 and Earlier Publications: There are several ways to purchase this material:
-Items listed on the registration form can be purchased with registration and picked up at the conference or mailed to you when available.
-Visit the ISSCC Publications Desk located in the registration area where you can pick up (or order for future delivery) materials from ISSCC 2017 and earlier conferences.
-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax.

HOW TO MAKE HOTEL RESERVATIONS

Online: Go to the conference website at www.isscc.org and click on the Hotel Reservation link for the SF Marriott Marquis ISSCC reservations website. **Conference room rates are $271 for a single/double, $296 for a triple and $321 for a quad.** ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**.
Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2017 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 12, 2017 to obtain the special ISSCC rates.

REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com Phone: 416-418-3034
Registration:	YesEvents 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2018 will be held on February 11-15, 2018 at the San Francisco Marriott Marquis Hotel.

Subcommittee Chairs

Analog:	Axel Thomsen
Data Converters:	Un-Ku Moon
Digital Architectures & Systems:	Byeonggyu Nam
Digital Circuits:	Edith Beigné
Imagers, MEMS, Medical & Displays:	Makoto Ikeda
Memory:	Leland Chang
RF:	Piet Wambacq
Technology Directions:	Eugenio Cantatore
Wireless:	Aarno Pärssinen
Wireline:	Frank O'Mahony

Program-Committee Chair: Boris Murmann
Program-Committee Vice-Chair: Alison Burdett
Conference Chair: Anantha Chandrakasan

ISSCC 2017 Papers at a Glance

Session 1, Monday Morning February 6th
Sessions 2-6, Monday Afternoon February 6th
Sessions 7-12, Tuesday Morning February 7th
Sessions 13-17, Tuesday Afternoon February 7th
Sessions 18-23, Wednesday Morning February 8th
Sessions 24-29, Wednesday Afternoon February 8th

Session 1 - Plenary

1.1 **A Smart Design Paradigm for Smart Chips**
Cliff Hou, *Vice President, Research & Development, TSMC, Hsinchu, Taiwan*

1.2 **Dynamics of Exponentials in Circuits and Systems**
Ahmad Bahai, *Chief Technology Officer, Texas Instruments, Santa Clara, CA*

1.3 **The Development of High-Speed DNA Sequencing: Jurassic Park, Neanderthal, Moore, and You**
Jonathan Rothberg, *Founder, 4Catalyzer and Adjunct Professor of Genetics, Yale School of Medicine, New Haven, CT*

1.4 **Quantum Computing – The Next Challenge in Circuit and System Design**
Lieven Vandersypen, *Antoni van Leeuwenhoek Professor, QuTech and Kavli Institute of NanoScience, TU Delft, The Netherlands*

Session 2 - Power Amplifiers

2.1 **A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications,** *Georgia Institute of Technology*

2.2 **A Fully Integrated Reconfigurable Wideband Envelope-Tracking SoC for High-Bandwidth WLAN Applications in a 28nm CMOS Technology,** *Broadcom*

2.3 **A Single-Inductor Dual-Output Converter with Linear-Amplifier-Driven Cross Regulation for Prioritized Energy-Distribution Control of Envelope-Tracking Supply Modulator**
National Chiao Tung University; Realtek Semiconductor

2.4 **A 2.4V 23.9dBm 35.7%-PAE -32.1dBc-ACLR LTE-20MHz Envelope-Shaping-and-Tracking System with a Multi-Loop-Controlled AC-Coupling Supply Modulator and a Mode-Switching PA**
Hong Kong University of Science and Technology

2.5 **A High-Efficiency Multiband Class-F Power Amplifier in 0.153μm Bulk CMOS for WCDMA/LTE Applications,** *MediaTek*

2.6 **A SiGe BiCMOS E-Band Power Amplifier with 22% PAE at 18dBm OP_{1dB} and 8.5% at 6dB Back-Off Leveraging Current Clamping in a Common-Base Stage**
University of Pavia

2.7 **A Wideband 28GHz Power Amplifier Supporting 8×100MHz Carrier Aggregation for 5G in 40nm CMOS,** *Texas A&M University; Qualcomm*

2.8 **A Class-G Voltage-Mode Doherty Power Amplifier,** *University of California, San Diego*

Session 3 - Digital Processors

3.1 **POWER9™: A Processor Family Optimized for Cognitive Computing with 25Gb/s Accelerator Links and 16Gb/s PCIe Gen4,** *IBM*

3.2 **Zen: A Next-Generation High-Performance x86 Core,** *AMD*

3.3 **A 14nm 1GHz FPGA with 2.5D Transceiver Integration,** *Intel*

3.4 **A 10nm FinFET 2.8GHz Tri-Gear Deca-Core CPU Complex with Optimized Power-Delivery Network for Mobile SoC Performance,** *MediaTek; Endura Technologies*

3.5 **A 40nm Flash Microcontroller with 0.80μs Field-Oriented-Control Intelligent Motor Timer and Functional Safety System for Next-Generation EV/HEV,** *Renesas Electronics; Renesas System Design*

3.6 **A 60pJ/b 300Mb/s 128×8 Massive MIMO Precoder-Detector in 28nm FD-SOI,** *Lund University*

3.7 **A 1920×1080 30fps 2.3TOPS/W Stereo-Depth Processor for Robust Autonomous Navigation**
University of Michigan

Session 4 - Imagers

4.1 **A 640×480 Dynamic Vision Sensor with a 9μm Pixel and 300Meps Address-Event Representation**
Samsung Advanced Institute of Technology; Samsung Electronics

4.2 **A Fully Integrated CMOS Fluorescence Biochip for Multiplex Polymerase Chain-Reaction (PCR) Processes,** *InSilixa*

4.3 **A Programmable Sub-Nanosecond Time-Gated 4-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy,** *Shizuoka University*

4.4 **A Sub-nW 80mlx-to-1.26Mlx Self-Referencing Light-to-Digital Converter with AlGaAs Photodiode**
University of Michigan

4.5 **A 1.8e^-_{rms} Temporal Noise Over 110dB Dynamic Range 3.4μm Pixel Pitch Global Shutter CMOS Image Sensor with Dual-Gain Amplifiers, SS-ADC and Multiple-Accumulation Shutter,** *Canon*

4.6 **A 1/2.3in 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM**
Sony Semiconductor Solutions; Sony Semiconductor Manufacturing; Sony LSI Design

4.7 **A 2.1Mpixel Organic-Film Stacked RGB-IR Image Sensor with Electrically Controllable IR Sensitivity,** *Panasonic*

4.8 **A 0.44e^-_{rms} Read-Noise 32fps 0.5Mpixel High-Sensitivity RG-Less-Pixel CMOS Image Sensor Using Bootstrapping Reset,** *Shizuoka University; Brookman Technology*

4.9 **A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing,** *Sony Semiconductor Solutions; Sony LSI Design; University of Tokyo*

Session 5 - Analog Techniques

5.1 **A 5x80W 0.004%-THD+N Automotive Multiphase Class-D Audio Amplifier with Integrated Low-Latency ΔΣ ADCs for Digitized Feedback after the Output Filter**
NXP Semiconductors; Teledyne DALSA Semiconductors

5.2 **An 8Ω 10W 91%-Power-Efficiency 0.0023%-THD+N Multi-Level Class-D Audio Amplifier with Folded PWM,** *KAIST*

5.3 **A 95μW 24MHz Digitally Controlled Crystal Oscillator for IoT Applications with 36nJ Start-Up Energy and >13× Start-Up Time Reduction Using a Fully-Autonomous Dynamically Adjusted Load**
Holst Centre / imec

5.4 **Frequency-Locked-Loop Ring Oscillator with 3ns Peak-to-Peak Accumulated Jitter in 1ms Time Window for High-Resolution Frequency Counting,** *Texas Instruments*

5.5 **A Quadrature Relaxation Oscillator with a Process-Induced Frequency-Error Compensation Loop**
Pohang University of Science and Technology; Research Institute of Industrial Science & Technology

5.6 **A 0.68nW/kHz Supply-Independent Relaxation Oscillator with ±0.49%/V and 96ppm/C Stability**
ARM; University of Southampton

5.7 **A 19nV/√Hz-Noise 2μV-Offset 75μA Low-Drift Capacitive-Gain Amplifier with Switched-Capacitor ADC Driving Capability,** *Analog Devices*

5.8 **A 9.3nW All-in-One Bandgap Voltage and Current Reference Circuit**
Pohang University of Science and Technology

5.9 **An 18.75μW Dynamic-Distributing-Bias Temperature Sensor with 0.87°C(3σ) Untrimmed Inaccuracy and 0.00946mm^2 Area,** *TSMC*

5.10 **A 1A LDO Regulator Driven by a 0.0013mm^2 Class-D Controller,** *Marvell*

5.11 **A 65nm Inverter-Based Low-Dropout Regulator with Rail-to-Rail Regulation and over -20dB PSR at 0.2V Lowest Supply Voltage,** *Hong Kong University of Science and Technology*

Session 6 - Ultra-High-Speed Wireline

6.1 **A 56Gb/s PAM-4/NRZ Transceiver in 40nm CMOS,** *National Taiwan University*

6.2 **A 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology,** *University of California, Berkeley; Qualcomm Atheros*

6.3 **A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET**
Xilinx; University of California, Berkeley

6.4 **A 64Gb/s PAM-4 Transmitter with 4-Tap FFE and 2.26pJ/b Energy Efficiency in 28nm CMOS FDSOI**
STMicroelectronics; University of Pavia

6.5 **A 1.8pJ/b 56Gb/s PAM-4 Transmitter with Fractionally Spaced FFE in 14nm CMOS**
IBM T. J. Watson Research Center

6.6 **A 22.5-to-32Gb/s 3.2pJ/b Referenceless Baud-Rate Digital CDR with DFE and CTLE in 28nm CMOS**
University of Toronto; Fujitsu Laboratories

6.7 **A 28Gb/s Digital CDR with Adaptive Loop Gain for Optimum Jitter Tolerance**
University of Toronto; Fujitsu Laboratories

Session 7 - Wireless Transceivers

7.1 **An 802.11ac Dual-Band Reconfigurable Transceiver Supporting up to Four VHT80 Spatial Streams with 116fs_{rms}-Jitter Frequency Synthesizer and Integrated LNA/PA Delivering 256QAM 19dBm per Stream Achieving 1.733Gb/s PHY Rate,** *MediaTek*

7.2 **A 28GHz 32-Element Phased-Array Transceiver IC with Concurrent Dual Polarized Beams and 1.4 Degree Beam-Steering Resolution for 5G Communication**
IBM T. J. Watson Research Center; Ericsson; IBM Research

7.3 **A 40nm Low-Power Transceiver for LTE-A Carrier Aggregation,** *MediaTek*

7.4 **A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm^3 Wireless Sensor Node with 20m Non-Line-of-Sight Communication**
University of Michigan; CubeWorks

7.5 **A TCXO-less 100Hz-Minimum-Bandwidth Transceiver for Ultra-Narrow-Band sub-GHz IoT Cellular Networks,** *CEA-LETI-MINATEC; Sigfox*

7.6 **A +8dBm BLE/BT Transceiver with Automatically Calibrated Integrated RF Bandpass Filter and -58dBc TX HD2,** *MediaTek*

7.7 **A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS,** *Novelda; University of Oslo*

Session 8 - Digital PLLs and Security Circuits

8.1 **Improved Power-Side-Channel-Attack Resistance of an AES-128 Core via a Security-Aware Integrated Buck Voltage Regulator,** *Georgia Institute of Technology; Intel*

8.2 **8Mb/s 28Mb/mJ Robust True-Random-Number Generator in 65nm CMOS Based on Differential Ring Oscillator with Feedback Resistors,** *Pohang University of Science and Technology*

8.3 **A 553F^2 2-Transistor Amplifier-Based Physically Unclonable Function (PUF) with 1.67% Native Instability,** *University of Michigan*

8.4 **A 2.5ps 0.8-to-3.2GHz Bang-Bang Phase- and Frequency-Detector-Based All-Digital PLL with Noise Self-Adjustment,** *University of Michigan; Seoul National University*

8.5 **A 0.42ps-Jitter -241.7dB-FOM Synthesizable Injection-Locked PLL with Noise-Isolation LDO**
Tokyo Institute of Technology

8.6 **A 2.5-to-5.75GHz 5mW 0.3ps_{rms}-Jitter Cascaded Ring-Based Digital Injection-Locked Clock Multiplier in 65nm CMOS,** *University of Illinois*

8.7 **A 0.0047mm^2 Highly Synthesizable TDC- and DCO-Less Fractional-N PLL with a Seamless Lock-Range of f_{REF} to 1GHz,** *Pohang University of Science and Technology; Samsung Electronics*

Session 9 - Sensors

9.1 **A Resistor-Based Temperature Sensor with a 0.13pJ·K^2 Resolution FOM**
Delft University of Technology; Ulm University; Broadcom

9.2 **A 0.6nJ -0.22/+0.19°C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence,** *University of Michigan*

9.3 **A BJT-Based Temperature Sensor with a Packaging-Robust Inaccuracy of ±0.3°C (3σ) from -55°C to +125°C After Heater-Assisted Voltage Calibration,** *Delft University of Technology*

9.4 **A 27μW 0.06mm^2 Background Resonance Frequency Tuning Circuit Based on Noise Observation for a 1.71mW CT-ΔΣ MEMS Gyroscope Readout System with 0.9°/h Bias Instability**
University of Freiburg - IMTEK; Hahn-Schickard

9.5 **A 1.8V True-Differential 140dB SPL Full-Scale Standard CMOS MEMS Digital Microphone Exhibiting 67dB SNR,** *Infineon Technologies*

9.6 **A 3.9kHz-Frame-Rate Capacitive Touch System with Pressure/Tilt Angle Expressions of Active Stylus Using Multiple-Frequency Driving Method for 65" 104×64 Touch Screen Panel**
Hanyang University; Leading UI; Chung-Ang University; MiraeTNS

9.7 **A 6.9mW 120fps 28×50 Capacitive Touch Sensor with 41.7dB SNR for 1mm Stylus Using Current-Driven ΔΣ ADCs,** *Yonsei University; TRAIS*

9.8 **An Energy-Efficient 3.7nV/√Hz Bridge-Readout IC with a Stable Bridge Offset Compensation Scheme**
Delft University of Technology

9.9 **A 0.6nm Resolution 19.8mW Eddy-Current Displacement Sensor Interface with 126MHz Excitation**
Delft University of Technology; Catena Microelectronics

Session 10 - DC-DC Converters

10.1 **A 1.1W/mm^2-Power-Density 82%-Efficiency Fully Integrated 3:1 Switched-Capacitor DC-DC Converter in Baseline 28nm CMOS Using Stage Outphasing and Multiphase Soft-Charging**
KU Leuven

10.2 **A Digitally Controlled 94.8%-Peak-Efficiency Hybrid Switched-Capacitor Converter for Bidirectional Balancing and Impedance-Based Diagnostics of Lithium-Ion Battery Arrays**
Dartmouth College; Intel; Hive Battery Management

10.3 **A 94.2%-Peak-Efficiency 1.53A Direct-Battery-Hook-Up Hybrid Dickson Switched-Capacitor DC-DC Converter with Wide Continuous Conversion Ratio in 65nm CMOS,** *University of Illinois*

10.4 **A Hybrid Inductor-Based Flying-Capacitor-Assisted Step-Up/Step-Down DC-DC Converter with 96.56% Efficiency,** *KAIST*

10.5 **A Three-Level Single-Inductor Triple-Output Converter with an Adjustable Flying-Capacitor Technique for Low Output Ripple and Fast Transient Response**
National Chiao Tung University; Realtek Semiconductor

10.6 **A 30MHz Hybrid Buck Converter with 36mV Droop and 125ns 1% Settling Time for a 1.25A/2ns Load Transient,** *Hong Kong University of Science and Technology*

10.7 **A 25MHz 4-Phase SAW Hysteretic DC-DC Converter with 1-Cycle APC Achieving 190ns t_{settle} to 4A Load Transient and Above 80% Efficiency in 96.7% of the Power Range**
University of Texas at Dallas

10.8 **A Buck Converter with 240pW Quiescent Power, 92% Peak Efficiency and a 2×10^6 Dynamic Range**
IBM T. J. Watson Research Center; Massachusetts Institute of Technology

Session 11 - Nonvolatile Memory Solutions

11.1 **A 512Gb 3b/Cell Flash Memory on 64-Word-Line-Layer BiCS Technology,** *Western Digital; Toshiba*

11.2 **A 1Mb Embedded NOR Flash Memory with 39μW Program Power for mm-Scale High-Temperature Sensor Nodes,** *University of Michigan; TSMC*

11.3 **A 10nm 32Kb Low-Voltage Logic-Compatible Anti-Fuse One-Time-Programmable Memory with Anti-Tampering Sensing Scheme,** *TSMC Design Technology*

11.4 **A 512Gb 3b/cell 64-Stacked WL 3D V-NAND Flash Memory,** *Samsung Electronics*

Session 12 - SRAM

12.1 **A 7nm 256Mb SRAM in High-K Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-V_{MIN} Applications,** *TSMC Design Technology; TSMC*

12.2 **A 7nm FinFET SRAM Macro Using EUV Lithography for Peripheral Repair Analysis**
Samsung Electronics

12.3 **A Low-Power and High-Performance 10nm SRAM Architecture for Mobile Applications**
TSMC Design Technology

12.4 **1.4Gsearch/s 2Mb/mm^2 TCAM Using Two-Phase-Precharge ML Sensing and Power-Grid Pre-Conditioning to Reduce Ldi/dt Power-Supply Noise by 50%**
Globalfoundries; Green Mountain Semiconductor; IBM Research; ASIC North

Session 13 - High-Performance Transmitters

13.1 **A Fully Integrated Multimode Front-End Module for GSM/EDGE/TD-SCDMA/TD-LTE Applications Using a Class-F CMOS Power Amplifier,** *MediaTek*

13.2 **A Digital Multimode Polar Transmitter Supporting 40MHz LTE Carrier Aggregation in 28nm CMOS**
Intel; DPMA; DMCE

13.3 **A SAW-less Reconfigurable Multimode Transmitter with a Voltage-Mode Harmonic-Reject Mixer in 14nm FinFET CMOS,** *Samsung Semiconductor; Samsung Electronics*

13.4 **All-Digital RF Transmitter in 28nm CMOS with Programmable RX-Band Noise Shaping**
Aalto University; Huawei Technologies

13.5 **A 0.35-to-2.6GHz Multilevel Outphasing Transmitter with a Digital Interpolating Phase Modulator Enabling up to 400MHz Instantaneous Bandwidth**
Aalto University; Tampere University of Technology; Nokia

13.6 **A 2.4GHz WLAN Digital Polar Transmitter with Synthesized Digital-to-Time Converter in 14nm Trigate/FinFET Technology for IoT and Wearable Applications**
Intel; Fudan University; Movellus Circuits; Radiawave Technologies

13.7 **A 0.23mm^2 Digital Power Amplifier with Hybrid Time/Amplitude Control Achieving 22.5dBm at 28% PAE for 802.11g,** *Marvell*

13.8 **A 24dBm 2-to-4.3GHz Wideband Digital Power Amplifier with Built-In AM-PM Distortion Self-Compensation,** *Georgia Institute of Technology; Intel*

13.9 **A 1.1V 28.6dBm Fully Integrated Digital Power Amplifier for Mobile and Wireless Applications in 28nm CMOS Technology with 35% PAE,** *Intel; University of Padova*

13.10 **A >1W 2.2GHz Switched-Capacitor Digital Power Amplifier with Wideband Mixed-Domain Multi-Tap FIR Filtering of OOB Noise Floor,** *Columbia University*

Session 14 - Deep-Learning Processors

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15.3 **An a-IGZO Asynchronous Delta-Sigma Modulator on Foil Achieving up to 43dB SNR and 40dB SNDR in 300Hz Bandwidth,** *Eindhoven University of Technology; Holst Centre / TNO*

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